Trusted Integrated Chips (TIC)

Obtaining World-Class Performance Without Compromising Security

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Split manufacturing eliminates the need to disclose the complete wiring plan for an integrated circuit outside the US

- Off-shore foundries lay down the transistor layer at the Front-End-Of-Line (FEOL) to obtain highest performance
- Chips come back to domestic foundries for metallization at the Back-End-Of-Line (BEOL) for security.
- Obfuscation techniques further protect sensitive chip designs

Over 90% of the world’s foundry capacity is controlled by non-U.S. companies with the vast majority of it located in Asia.

How to use it without compromising design security?

Logic families covered in TIC include: photonics, mixed-signal CMOS, analog, digital and RRAM, and sonic MEMS

TIC is also advancing “More-Than-Moore” technology to foster cutting-edge capabilities in the U.S.

Carnegie Mellon University

Stanford

Raytheon

Cornell University

Brokerage services by MOSIS

Technical coordination by Sandia National Laboratories

Independent test and evaluation by USC/ISI and MOSIS

65 nm results – April 2014

No statistically significant difference in electrical performance characteristics

TIC 65nm MPW-1 300 mm Wafer, Global Foundries / IBM

65 nm results – April 2014 fabricated jointly between Global Foundries (Singapore) and IBM (East Fishkill)

1 TSMC Taiwan 51.0%
2 Global Foundries Singapore, Germany 11.1%
3 Samsung Korea 10.3%
4 UMC Taiwan, Singapore 10.1%
5 SMIC China 5.2%
6 Powerchip Taiwan 3.1%
7 Vangard Taiwan 1.8%
8 Huahong Grace China 1.8%
9 Dongbu Korea 1.5%
10 TowerJazz Israel 1.3%
11 IBM USA 1.0%
12 MagnaChip Korea 1.0%

2013 Worldwide Semiconductor Foundry Production

TIC program timeline

130 nm results – March 2013

CMU = Carnegie Mellon University

RVS = Raytheon Vision Systems