



# Trusted Integrated Chips (TIC)

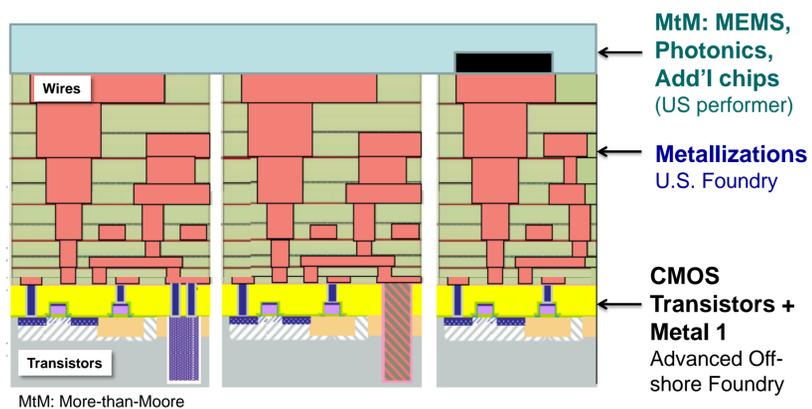
Obtaining World-Class Performance Without Compromising Security

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Split manufacturing eliminates the need to disclose the complete wiring plan for an integrated circuit outside the US

- Off-shore foundries lay down the transistor layer at the Front-End-Of-Line (FEOL) to obtain highest performance
- Chips come back to domestic foundries for metallization at the Back-End-Of-Line (BEOL) for security.
- Obfuscation techniques further protect sensitive chip designs



Logic families covered in TIC include: photonics, mixed-signal CMOS, analog, digital and RRAM, and sonics MEMS

TIC is also advancing "More-Than-Moore" technology to foster cutting-edge capabilities in the U.S.



Carnegie Mellon University



Stanford

Raytheon



Cornell University

Brokerage services by MOSIS

Technical coordination by Sandia National Laboratories

Independent test and evaluation by USC/ISI and MOSIS

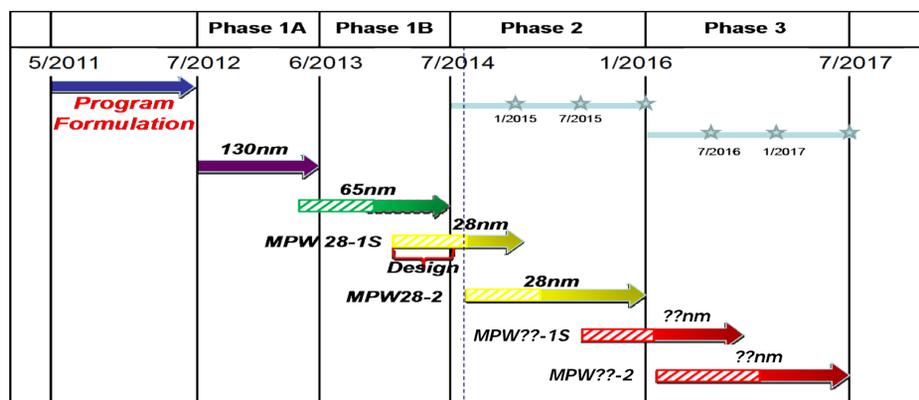
Over 90% of the world's foundry capacity is controlled by non-U.S. companies with the vast majority of it located in Asia. How to use it without compromising design security?



2013 Worldwide Semiconductor Foundry Production

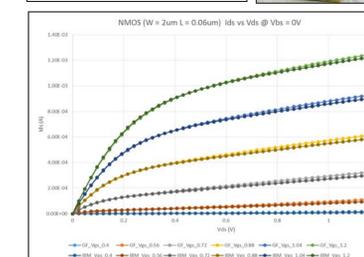
1	TSMC	Taiwan	51.0%	7	Vanguard	Taiwan	1.8%
2	Global Foundries	Singapore, Germany	11.1%	8	Huahong Grace	China	1.8%
3	Samsung	Korea	10.3%	9	Dongbu	Korea	1.5%
4	UMC	Taiwan, Singapore	10.1%	10	TowerJazz	Israel	1.3%
5	SMIC	China	5.2%	11	IBM	USA	1.0%
6	Powerchip	Taiwan	3.1%	12	MagnaChip	Korea	1.0%

## TIC program timeline

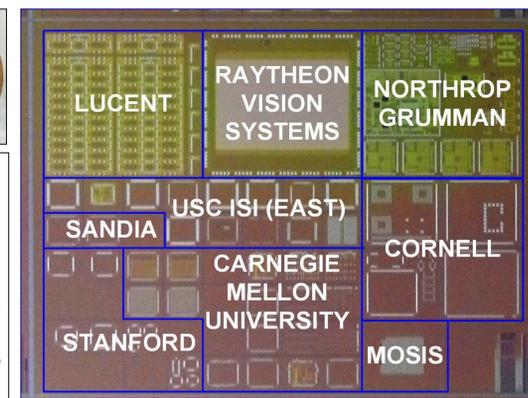


## 65 nm results – April 2014

TIC 65nm MPW-1 300 mm Wafer Global Foundries / IBM



No statistically significant difference in electrical performance characteristics



IARPA multi-user test chip April 2014 fabricated jointly between Global Foundries (Singapore) and IBM (East Fishkill)

Metrics		OY 1 (12 mo)	CMU	Cornell	LGS/Bell Labs	RVS	Stanford
Technology Node		65 nm node	65 nm node	65 nm node	65 nm node	65 nm node	65 nm node
Circuit Complexity (# of transistors)	Digital	>100K	>1M	3400K	>600K	65300K	>100K
	Analog/Mixed Signal	>1K	>5K	>30K	1.8K	1310K	na
Split-Fabrication Yield		>75%	100%	100%	100%	100%	100%
Speed		>80%	102%	95%	100%	89%	100%
Power Dissipation		<125%	104%	105%	100%	105%	100%

CMU = Carnegie Mellon University  
RVS = Raytheon Vision Systems

## 130 nm results – March 2013

Metrics		Base (12 mo)	CMU	Cornell	LGS/Bell Labs	RVS	Stanford
Technology Node		130 nm node	130 nm node	130 nm node	130 nm node	130 nm node	130 nm node
Circuit Complexity (# of transistors)	Digital	>10K	>100K	1300K	10K	5050K	>20K
	Analog/Mixed Signal	>100	>1K	>18K	1.8K	74K	na
Split-Fabrication Yield		>50%	100%	98%	90%	94%	100%
Speed		>70%	104%	95%	125%	100%	100%
Power Dissipation		<150%	104%	105%	100%	100%	100%