

OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE



**SuperTools
Proposers' Day Brief
Office of Safe and Secure Operations**

**Mark Heiligman
Program Manager**

10 February 2016

INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)



SuperTools Program Proposers' Day Agenda

Time	Topic	Speaker
9:00 am – 9:30 am	Registration and Check In	
9:30 am – 9:45 am	IARPA Overview and Remarks	Bill Vanderlinde Office Director
9:45 am – 10:30 am	SuperTools Program Overview	Mark Heiligman Program Manager
10:30 am – 11:00 am	BAA Overview, T&E, GFI/GFE	Mark Heiligman Program Manager
11:00 am – 11:30 am	Break	
11:30 am – 12:00 pm	Doing Business with IARPA	Tarek Abboushi IARPA Acquisition
12:00 pm – 12:30 pm	SuperTools Program Questions & Answers	Mark Heiligman Program Manager
12:30 pm – 1:30 pm	Lunch	
1:30 pm – 3:00 pm	Proposers' 5-minute Capability Presentations	Attendees (No Government)
3:00 pm – 4:00 pm	Proposers' Networking and Teaming Discussions	Attendees (No Government)



Proposers' Day Goals

- Familiarize participants with IARPA and with the SuperTools program concept.
- Solicit feedback and questions.
- Foster networking and discussion of synergistic opportunities and capabilities among potential program participants (A.K.A. “teaming”).
- Please ask questions and make suggestions: this is your chance to influence the design of the program.
 - We appreciate and seek constructive feedback on any / all aspects of the program design and program metrics.
 - Record your questions and comments on the note cards provided and submit them to IARPA staff during the break.
 - After today, questions will be answered in writing on the program website.
- Once a BAA is released, questions can only be submitted to the email address provided in the BAA.



Disclaimer

- These presentations are provided solely for information and planning purposes.
- The Proposers' Day does not constitute a formal solicitation for proposals or abstracts.
- Nothing said at Proposers' Day changes the requirements set forth in a BAA.
 - A BAA supersedes anything presented or said by IARPA at the Proposers' Day.

OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE



IARPA Overview

William Vanderlinde, PhD
Office Director, Safe and Secure Operations
IARPA

INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)



Office of the Director of National Intelligence

Central Intelligence Agency

Defense Intelligence Agency

Department of State

National Security Agency

Department of Energy

National Geospatial-Intelligence Agency

Department of the Treasury

National Reconnaissance Office

Drug Enforcement Administration

Army

Federal Bureau of Investigation

Navy

Department of Homeland Security

Air Force

Coast Guard

Marine Corps





IARPA Mission and Method

IARPA's mission is to invest in high-risk/high-payoff research to provide the U.S. with an overwhelming intelligence advantage

- **Bring the best minds to bear on our problems**
 - Full and open competition to the greatest possible extent
 - World-class, rotational Program Managers
- **Define and execute research programs that:**
 - Have goals that are clear, measureable, ambitious and credible
 - Employ independent and rigorous Test & Evaluation
 - Involve IC partners from start to finish
 - Run from three to five years
 - Publish peer-reviewed results and data, to the greatest possible extent



Analysis R&D

“Maximizing insight from the information we collect, in a timely fashion”

Large Data Volumes and Varieties

Providing powerful new sources of information from massive, noisy data that currently overwhelm analysts

Social, Cultural, and Linguistic Factors

Analyzing language and speech to produce insights into groups and organizations

Improving Analytic Processes

Dramatic enhancements to analytic process at the individual and group level



Collection R&D

“Dramatically improve the value of collected data”

Novel Access

Reach hard targets in denied areas

Asset Validation and Identity Intelligence

Assess trustworthiness and advance biometrics in real-world conditions

Tracking and Locating

Accurately locate emitters and other intelligence interests



Anticipatory Intelligence R&D

“Detecting and forecasting significant events”

S & T Intelligence

Detecting and forecasting the emergence of new technical capabilities

Indications & Warnings

Early warning of social and economic crises, disease outbreaks, insider threats, and cyber attacks

Strategic Forecasting

Probabilistic forecasts of major geopolitical trends and rare events



Operations R&D

“Operate effectively in a globally interdependent and networked environment”

Computational Power

Revolutionary advances in science and engineering to solve problems intractable with today’s computers

Trustworthy Components

Gain the benefits of leading-edge hardware and software without compromising security

Safe and Secure Systems

Protecting systems against cyber threats



How to engage with IARPA

- **Website:** www.IARPA.gov
 - Reach out to us, especially the IARPA PMs. Contact information on the website.
 - Schedule a visit if you are in the DC area or invite us to visit you.
- **Opportunities to Engage:**
 - **Research Programs**
 - Multi-year research funding opportunities on specific topics
 - Proposers' Days are a great opportunity to learn what is coming, and to influence the program
 - **“Seedlings”**
 - Allow you to contact us with your research ideas at any time
 - Funding is typically 9-12 months; IARPA funds to see whether a research program is warranted
 - IARPA periodically updates the topics of interest
 - **Requests for Information (RFIs) and Workshops**
 - Often lead to new research programs, opportunities for you to provide input while IARPA is planning new programs



Concluding Thoughts

- **Our problems are complex and truly multidisciplinary**
- **Technical excellence & technical truth**
 - Scientific Method
 - Peer/independent review
 - Full and open competition
- **We are always looking for outstanding PMs**
- **How to find out more about IARPA:**

www.IARPA.gov
- **Contact Information**

Phone: 301-851-7500

OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE



SuperTools Program Overview

Mark Heiligman, PM
Office of Safe and Secure Operations

10 February 2016

INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)



Presentation Outline

- Motivation and Objectives
- Current Status
- Program Approaches
- BAA Overview
- Program Structure and Deliverables
- Technical Milestones and Program Metrics
- GFI/GFE and Test and Evaluation
- Reporting Requirements
- Schedule
- Management Plan and Teaming
- Proposal Evaluation Criteria
- Program Summary



SuperTools Bottom Line

- SuperTools seeks to enable very large scale integration (VLSI) design of superconducting electronics (SCE).
- SuperTools will develop a comprehensive set of Electronic design automation (EDA) tool-chain, Technology Computer Aided Design (TCAD) tools, and open/interoperable Cell Library standards.
- SuperTools will require a multi-disciplinary approach to leverage capability and expertise between industry and academia.



Motivation

- IARPA's portfolio in the high performance computing activity.
- Limitations of semiconductor based exascale computing
 - high power consumption and lower speed in CMOS based computing
- Superconducting Electronics (SCE) is a promising alternative technology with high switching speed and low power.



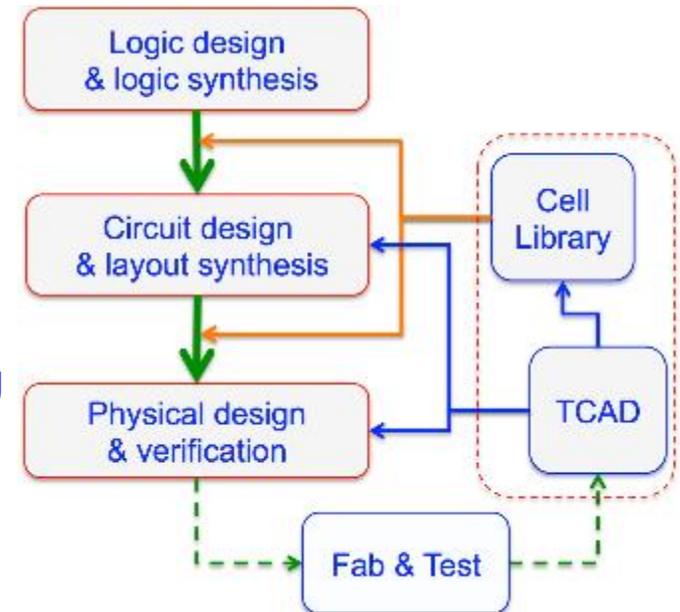
The Problem

- Gap in Technology for designing very large superconducting electronic circuits (e.g., microprocessors).
 - Electronic design automation (EDA) tool-chain and Technology CAD (TCAD) tools are incomplete or limited both in capability and scale.
- What we need:
 - A development path from a semi-automated tool chain to a fully automated and fully-functional tool chain for very large scale integration (VLSI) SCE design.



IC Design Workflow

- Model and simulate targeted design from functional/behavioral description at **logic design level** (RTL) with **HDL simulators**;
- Apply **automated logic synthesis** to produce (analog) **circuit schematics** (gate-level netlist) from a cell library of targeted **logic family and fab process**;
- Simulate, verify, and optimize resulting **circuit schematics** along with **clock and bias network** in **circuit design** stage before **layout synthesis** from the cell library;
- Perform (timing-driven) **automated placement and routing** on synthesized layout in **physical design** stage;
- Optimize and verify the physical layout with help of **parameter extraction tools**; and
- Tape out the physical layout for **fabrication and test**.



HDL = Hardware Description Language
RTL = Register Transfer Level



SCE EDA & TCAD Tools

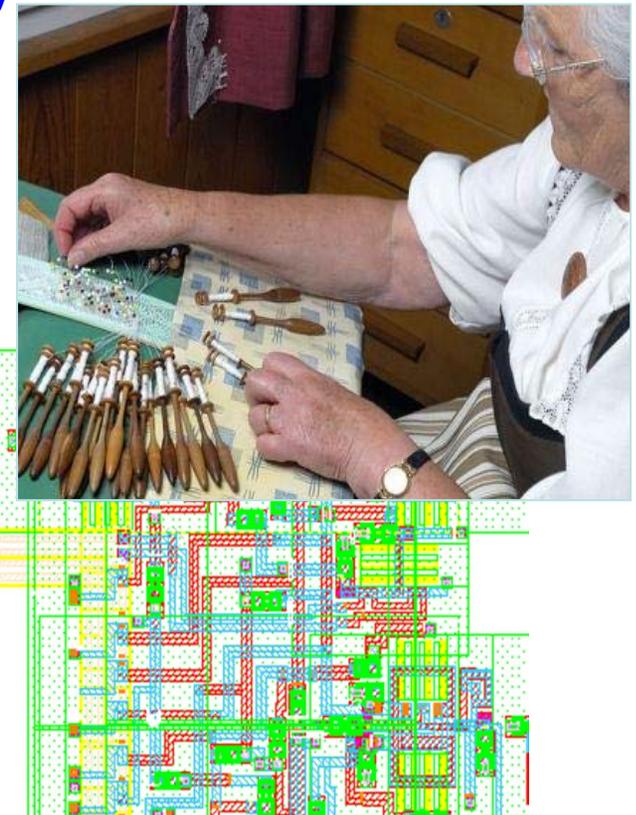
- Logic/digital design tools and HDL simulators.
- Logic synthesis tools.
- Clock tree and bias network synthesis tools (or integrated into synthesis tools).
- Analog circuit schematic simulator and editor.
- Layout synthesis tool and editor.
- Place-and-route tools.
- Physical design verification tools.
- Physics-based device and process simulation tools, and compact models of circuit elements and electromagnetic environment.
- Device and circuit parameter extraction tools.
- Common templates of Standard Cell Library (for digital, analog and layout synthesis and simulations).
- Timing, power, and thermal analysis tools

HDL = Hardware Description Language
RTL = Register Transfer Level



How Is It Done Today?

- Logic and circuit elements in synthesis stages are **manually** input, replaced, and modified.
- **Manually place-and-route** elements in layout stages.
- Several EDA tools are missing or needing improvement:
 - Inductance extraction,
 - Placement and routing,
 - **Design automation and synthesis tools**,
 - New **timing-aware** circuit description methods,
 - Design algorithms for **timing-driven optimization**, and
 - **Standardized benchmarking** designs for comparison of processes, cell libraries, and tool-chains.



“Manual design is like making lace.” (SFQ designer)



Program Objectives

SuperTools seeks to

- Develop a comprehensive set of **Electronic Design Automation (EDA) tools** to enable **Very-Large-Scale Integration (VLSI) design** of **Superconducting Electronics (SCE)** from HDL to GDSII,
- Develop physics-based **Technology CAD (TCAD) tools** to enable device and process simulations and device parameter extractions for better design-to-hardware fidelity, and
- Establish **open, interoperable Standard Cell Library formats** as standardized interface to bridge collaboration between foundry and designers and to speed up technology development.

Target SCE design capability:

- Phase I: support design of circuits with **>100k JJs** (or 10k gates)
- Phase II: support design of circuits with **>1M JJs** (or 100k gates)
- Phase III: support design of circuits with **>10M JJs** (or 1M gates)



Challenges

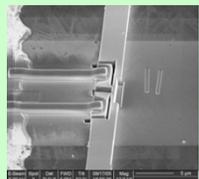
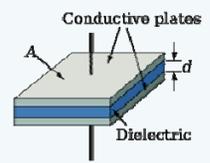
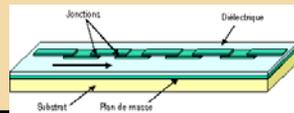
SCE versus CMOS

- Different representation of logic states and switch construct: SCE pulse logic vs. CMOS level logic.
- Different switch construct: Single Flux Quantum (SFQ) vs. Field Effect Transistor (FET).
- Different timing/clocking and distribution schemes.
- Different biasing and distribution schemes.
- Different suites of basic logic gates and constructs.
- Different types of inter-gate influence: magnetic vs. electric coupling.
- Different passive components: inductor vs. capacitor (current vs. charge).
- Different interconnect technology: superconductor vs. normal conductor
- Existence of non-logic SCE cells: interconnects (JTLs, PTLs), asynchronous components (splitter, merger), and other special purpose circuits (SFQ/DC and DC/SFQ converters).

SCE vs CMOS: Physics and Construct

- Design tools developed for conventional electronics are not able to handle differences in superconducting circuits, including:

At the circuit and physical levels

	CMOS	SCE
Active component	Transistor (V) 	Josephson Junction (ϕ) 
Passive component	Capacitor (C) 	Inductor (L) 
Interconnect	Normal Conductor (R) 	Superconductor ($R = 0$) 

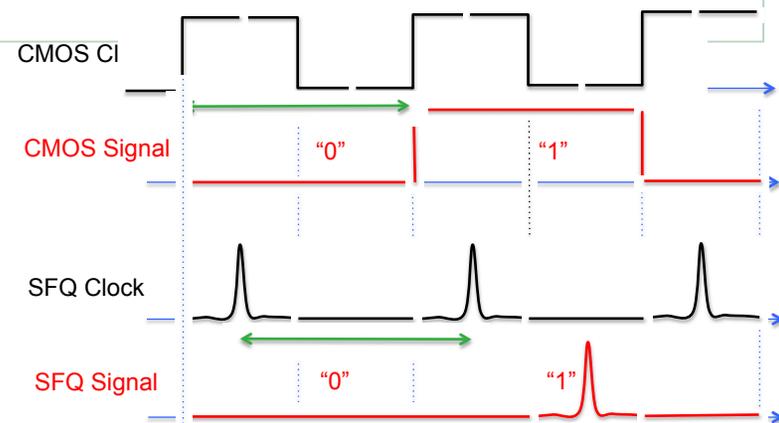


SCE vs CMOS: Logic and Construct

- Design tools developed for conventional electronics are not able to handle differences in superconducting circuits, including:

At the logic and system levels

- Different representation of **logic states (voltage-levels vs. pulses)**
- Different suite of **basic logic gates and constructs**
- Different **synchronization** and **biasing** schemes
- Different levels of **inter-gate influence** (magnetic vs. electric coupling)
- Non-logic SCE elements

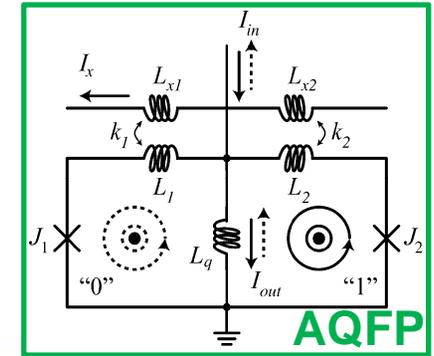
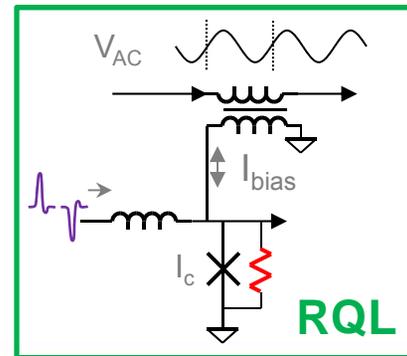
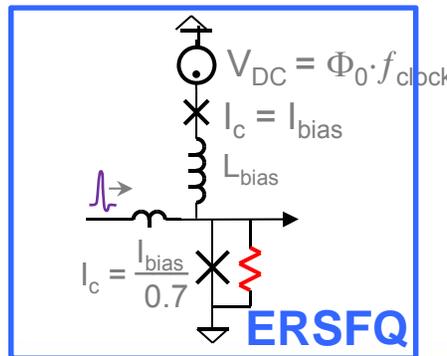
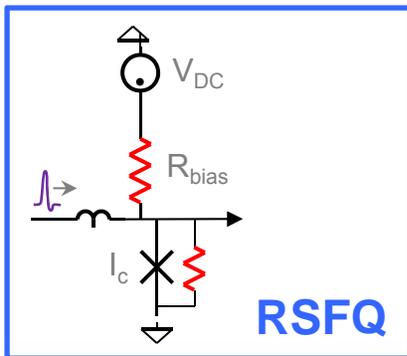




SCE Logic Families and Basic Cells

- SFQ logic families
 - DC-biased logic: RSFQ, eRSFQ, eSFQ.
 - AC-biased logic: RQL, AQFP.
- SFQ basic cells
 - Logic: AND, OR, inverter, XOR, AND/OR, etc.
 - Storage: DFF, TFF, memory cells, etc.
 - Interconnects: JTL, PTL+RX/TX.
 - Asynchronous components: merger, splitter, CB etc.
 - Special purpose circuits: SFQ/DC, DC/SFQ converters, etc.

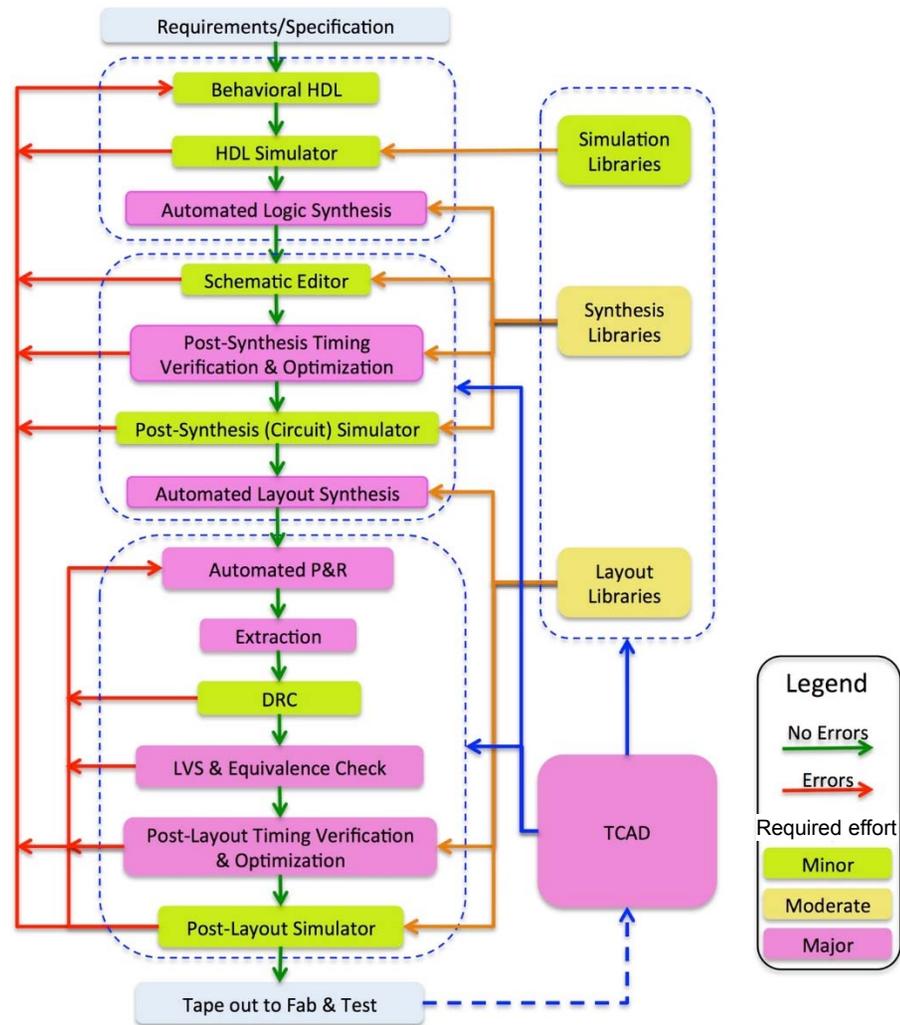
SFQ = Single Flux Quantum,
 RSFQ = Rapid Single Flux Quantum,
 RQL = Reciprocal Quantum Logic,
 AQFP = Adiabatic Quantum Flux Parametron,
 eRSFQ = Energy-efficient Rapid Single Flux Quantum,
 eSFQ = Efficient Single Flux Quantum,
 JTL = Josephson (Junction) Transmission Line,
 PTL+RX/TX = Passive Transmission Line with receiver and driver
 DFF = D-type (Data) Flip-Flop
 TFF = Toggle Flip-Flop
 CB = Confluence Buffer





SCE EDA Tool Status

- Design, analysis, and verification tools need to be developed into a comprehensive EDA tool set specific to **very large scale superconducting integrated circuits**.

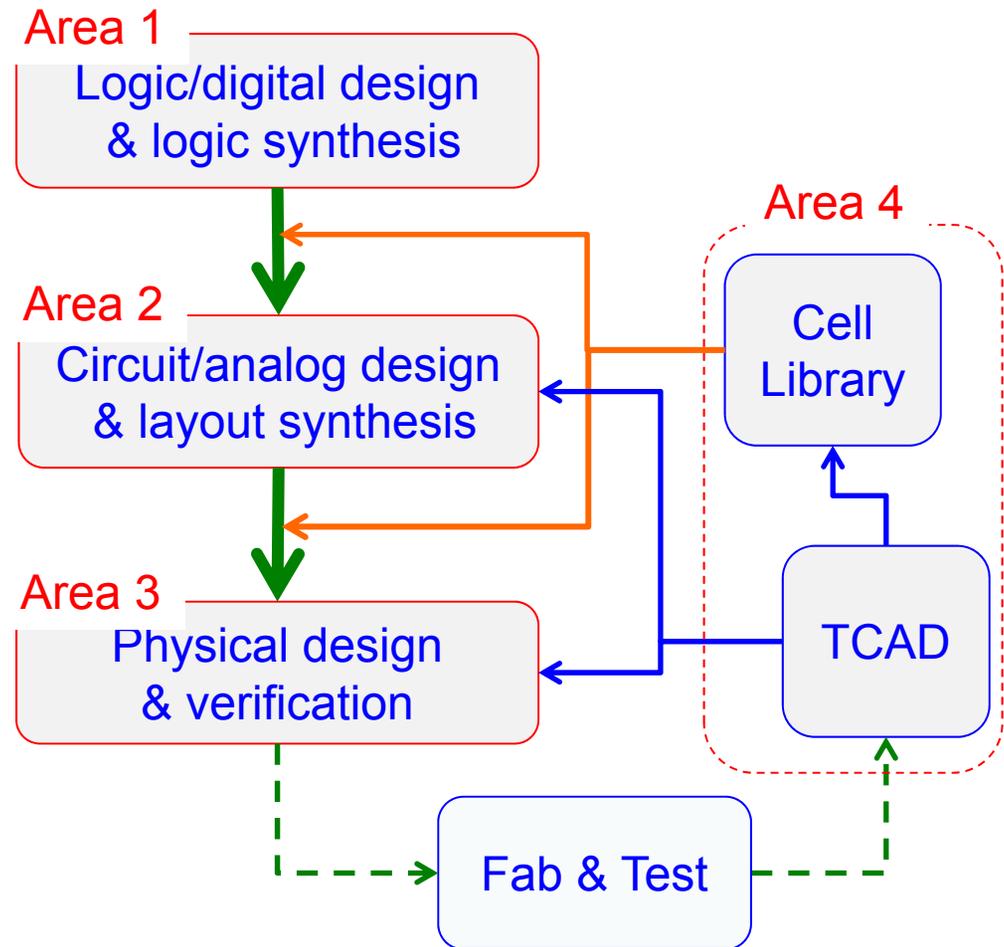


HDL = Hardware Description Language
P&R = Place-and-Route
DRC = Design Rule Check
LVS = Layout versus Schematic
TCAD = Technology CAD



SuperTools Approach

- To concurrently focus on Four Program Focus Areas, addressing:
 - Each major step of the EDA design flow, and
 - Back-end support with development of Cell Library standards & TCAD tools.
- To incorporate SCE-Specific design considerations and features into tool development.





SCE Specific Design Considerations

- Multiple logic families
- Timing/clocking scheme and distribution (**critical**)
- Biasing scheme and distribution
- Limited fan-out of the gates (need splitters)
- Interconnects are not free (need JJs for JTLs, PTLs, and cross-over cells)).
- Non-linearity of Josephson junctions (current and phase dependence in SFQ/JJ-SIM models)
- Inherent pipelined architecture for SFQ gates and memory elements
- State read-out operations are mostly destructive
- Different suite of preferred logic primitives in SCE than CMOS
- Parasitic magnetic coupling (mutual inductance between elements)
- Flux trapping prevention
- Potential bias current redistribution between cells if not done properly



Target Tool Features

- Support **multiple families of single flux quantum (SFQ) digital logic** (DC- and AC-biased logic constructs).
- Allow circuit design with **multiple timing schemes** (synchronous, asynchronous and mixed architecture).
- Support **design optimization** based on metrics such as circuit area, power, energy per operation, number of gates, or speed.
- Applicable to **clock speeds** of 100 GHz or greater.
- Compatible with an existing CMOS tool chain for **hybrid integration**.
- Support **a common Standard Cell Library format**.
(Similar to open/inter-operable Process Development Kits (OpenPDK/iPDK) and each foundry only needs to provide one standardized set to IC designers without potentially lossy data conversion or scripting.)



Overview of Program Focus Areas

SuperTools consists of four program focus areas, addressing each major step of the EDA design flow and back-end support (Cell Library & TCAD):

Logic/digital Design

Simulations, verification, and automated logic synthesis in the HDL/RTL (digital) level.

Circuit/analog Design

Simulations, verification, and automated layout synthesis in the circuit schematic (analog) level.

Physical Design

Automated physical layout and extraction-verification.

TCAD and Library

Development of (physics-based) TCAD tools and open/interoperable Standard Cell Library standards.



BAA Overview, T&E, GFI/GFE



BAA Highlights

- Concurrent development of all four program focus areas
 - EDA tool chain (Digital, Analog, and Physical Design)
 - TCAD tools and Cell Library standards
- Program duration: 5 years in 3 phases
 - Phase I: 2 years
 - Phase II: 2 years
 - Phase III: 1 year
- Technical Milestones for each 6 month period after the first year.
- Metrics and objectives for each phase.



SuperTools Timeline



- Initial tool development so as to acquire missing tools and extend existing CMOS-based tools.
- Draft requirements and formats of Standard Cell Library.

- Improve and increase the capability of tools.
- Establish Standard Cell Library standards.
- Automate the full design flow with standardized interface for all logic families and timing schemes.
- Test device fabrication and measurement for model calibrations.

- Improve usability and establish interface to other technologies for full system integration.
- Integrate and optimize the tool-chain, and further increase its capabilities.



Program Structure Overview

- **Phase I: Initial tool development**
 - Develop missing tool capabilities to enable VLSI SCE design.
 - Draft requirements and formats of open/interoperable Standard Cell Library.
 - Design capability target: **100k JJs, or 10k gates.**
- **Phase II: Tool improvement**
 - Improve and increase the capability of EDA and TCAD tools, and compact models.
 - Establish standards for an open/interoperable Standard Cell Library.
 - Automate the full design flow and establish standardized interface for all logic families and timing schemes.
 - Test device fabrication and measurement for model calibrations.
 - Design capability target: **1M JJs, or 100k gates.**
- **Phase III: Tool integration and capability extension**
 - Improve usability and establish interface to other technologies for full system integration.
 - Integrate and optimize the tool-chain, and further increase its capabilities.
 - Design capability target: **10M JJs, or 1M gates.**



Program Structure: Phase I

Phase I: Initial Tool Development (Part I-1)

- Overview

- Initial tool development so as to acquire missing tools and extend existing CMOS-based tools.
 - Target capability: >100 k JJs (or >10k gates) suitable for 32-bit RISC processor level design.
- Draft requirements and formats of Standard Cell Library.

- Logic design tool development

- Extend HDL/logic simulators to handle SCE-specific feature of logic elements with timing analysis.
- Develop automated logic synthesis tool subject to timing and/or biasing constraints for both synchronous and asynchronous architecture.

...



Program Structure: Phase I *cont.*

Phase I: Initial Tool Development (Part I-2)

- **Circuit design tool development**
 - Extend circuit schematic simulator to handle SCE specific feature in circuit elements with timing and biasing analysis.
 - Develop automated layout synthesis tool with clock and bias networks.
- **Physical design and verification tool development**
 - Develop automated placement and routing (P&R) tool driven by timing and/or biasing constraints, and post-layout timing analysis tool.
 - Build compact passive and parasitic parameter extraction tools (e.g. inductance extraction tool).
 - Produce Layout versus Schematics (LVS) or Equivalence Check tools.
 - Extend existing Design Rule Check (DRC) for SCE applications.



Program Structure: Phase I *cont.*

Phase I: Initial Tool Development (Part I-3)

- **Create Cell Library and cell templates**
 - Draft Standard Cell Library requirements and specifications with parameterized cell library entries for synchronous/asynchronous and DC/AC-biased logics.
 - Determine requirements of logic and circuit simulation parameters.
 - Establish a set (or sets) of generic cells for both logic and layout synthesis.
- **TCAD tool development**
 - Develop physics-based device simulation tool.
 - Extend process simulation tool to include SCE process flow and materials.
 - Develop compact models of circuit elements and electromagnetic environment (e.g. parasitic, crosstalk, magnetic coupling, etc.)
 - Develop or extend model parameter extraction tools suitable for SCE applications.



Program Structure: Phase II

Phase II: Tool Improvement (Part II-1)

- Overview

- Improve and increase the capability of tools.
 - Target capability: >1M JJs (or >100k gates) suitable for 32/64-bit RISC processor type design.
- Establish standards for an open/interoperable Standard Cell Library.
- Automate the full design flow and establish standardized interface for all logic families and timing schemes.

- Establishment of Standard Cell Library standards

- Create cell library standards scalable to more complex design and advanced technology nodes and compatible for multiple SFQ logic families and clocking schemes (with consensus from performers and T&E teams).
- Further extend the cell parameter sets to include process variations and noises.



Program Structure: Phase II *cont.*

Phase II: Tool Improvement (Part II-2)

- TCAD tool development and improvement
 - Improve physics-based device simulation tools with fab-assisted model calibration.
 - Improve process simulation tool with fab-assisted model calibration.
 - Improve model parameter extraction tools with respect to extended requirements of Standard Cell Library.
 - Improve compact models of circuit elements and electromagnetic environment.
- Test device fabrication and measurement for model calibration
 - Coordinate with T&E teams to set up requirements for fab-assisted calibration.
 - Only to supplement data not available from other related programs or public domain.



Program Structure: Phase II *cont.*

Phase II: Tool Improvement (Part II-3)

- EDA tool improvement

- Extend tool capability to handle newly established Standard Cell Library standards.
- Enhance convergence of numerical solvers.
- Integrate TCAD-derived models into simulation tools for higher fidelity.
- Develop metric-driven optimization capability for synthesis and layout.
- Build capability to include margin, yield, and power analysis.



Program Structure: Phase III

Phase III: Tool Integration and Capability Extension (Part III-1)

- Overview

- Integrate and optimize the tool-chain, and further increase its capabilities.
 - Target capability: >10M JJs (or >1M gates) suitable for 64-bit RISC processor type design.
- Develop Integrated Development Environment (IDE) and enhance User Interface (UI).
- Develop interface for full system integration and other technologies, and develop associated analysis tools.

- TCAD tool enhancement

- Enhancement of compact device models.
- Improve device and process simulation tools with better fidelity and speed.



Program Structure: Phase III *cont.*

Phase III: Tool Integration and Capability Extension (Part III-2)

- EDA tool enhancement

- Develop Integrated Development Environment (IDE) for the EDA tool chain and improve User Interface (UI).
- Optimize EDA tools to increase fidelity and speed.
- Add Built-in Self-Test (BIST) and Design for Test (DFT) features.
- Develop hybrid integration capability to include non-SCE and memory elements.
- Develop interface to system integration and analysis tools.



Deliverables & Program Coordination

- **Deliverables**
 - EDA tool chain along with generic Standard Cell Library for T&E.
 - TCAD tools, and compact device models
 - Tool demonstration and instructions
 - Reports
- **Program Coordination**
 - SuperTools and C3 programs are to ensure data input and output requirements are compatible with performer capabilities.
 - Completed design modules are to be available to C3 performers for testing as part of a spiral development cycle.
 - SuperTools will allow feedback on functionality, models, parameter set, and usability from C3 performers.
 - SuperTools proposers are to provide recommendations on Government Purpose Rights (GPR) when incorporating existing software tools.



Out of Scope

- Methods or early research that has not yet demonstrate potential capability suitable for very large scale circuit design.
- Individual gadgets that cannot be integrated into a complete design flow.
- Manual or semi-automatic translations of CMOS design elements through tabulation or other similar mapping schemes.
- Proprietary formats of Standard Cell Library without public access or requiring licensing fees.



Technical Milestones

Month Milestones

Phase I (24 months): Initial Tool Development

- | Month | Milestones |
|-------|---|
| 12 | <ul style="list-style-type: none">• Demonstrate HDL/logic simulators to handle SCE-specific feature of logic elements with timing analysis.• Generate generic parameterized cell library for logic synthesis with extrapolated parameters and for both synchronous and asynchronous logic.• Demonstrate circuit simulator to handle SCE specific feature in circuit elements with timing analysis.• Generate parameterized cell library for layout synthesis (for both DC- and AC-biased logics).• Demonstrate process simulation tool to include SCE process flow and materials.• Demonstrate compact passive and parasitic circuit parameter extraction tools (for schematic simulation).• Generate compact models of circuit elements and electromagnetic environment. |

Milestones in BLUE are required, but deliverable dates within Phase I are flexible.



Technical Milestones

Month Milestones

Phase I (24 months): Initial Tool Development

- | | |
|----|--|
| 18 | <ul style="list-style-type: none">• Demonstrate automated logic synthesis tool with clock-tree and bias network synthesis capability.• Demonstrate automated layout synthesis tool with clock-tree and bias network synthesis capability.• Demonstrate clock and bias distribution analysis tools.• Demonstrate Design Rule Check (DRC) tool for SCE applications.• Demonstrate post-layout timing analysis tool.• Demonstrate Layout versus Schematics (LVS) or Equivalence Check tools. |
| 24 | <ul style="list-style-type: none">• Demonstrate automated placement and routing tool subject to timing and/or biasing constraints.• Demonstrate physics-based device simulation tool. |

Milestones in BLUE are required, but deliverable dates within Phase I are flexible.

After reaching milestones on the specified timeline, development of individual tools will continue in order to reach the overall 'end-of-phase' objectives.



Technical Milestones

Month	Milestones
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Phase II (24 months): Tool Improvement	
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- | | |
|----|--|
| 30 | <ul style="list-style-type: none">• Create a common standard for cell templates/formats scalable to more complex design and advanced technology nodes and compatible for multiple SFQ logic families (consensus from performers).• Generated enlarged parameter set to include process variations and noises. |
| 36 | <ul style="list-style-type: none">• Optimize process simulation tool with fab-assisted parameter calibration.• Improve compact models of circuit elements and electromagnetic environment.• Extend tool capability to handle the established Standard Cell Library formats. |

Performers and T&E teams are to set up requirements for fab-assisted calibration by month of 30.



Technical Milestones

Month	Milestones
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Phase II (24 months): Tool Improvement	
---	--

- | | |
|----|--|
| 42 | <ul style="list-style-type: none">• Extend and optimize model parameter extraction tools with respect to extended requirements of Standard Cell Library.• Demonstrate enhanced convergence of numerical solvers while extending the capability (scaling to higher # of JJs).• Demonstrate integrating TCAD-derived models into simulation tools for higher fidelity. |
| 48 | <ul style="list-style-type: none">• Demonstrate improved physics-based device simulation tool with fab-assisted parameter calibration.• Develop optimization capability for the synthesis and layout tools.• Demonstrate capability to include margin, power, yield, and thermal analysis. |



Technical Milestones

Month	Milestones
-------	------------

Phase III (12 months): Tool Integration and Capability Extension	
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- | | |
|----|---|
| 54 | <ul style="list-style-type: none">• Optimize the EDA tools to increase fidelity and speed.• Add Built-in Self-Test (BIST) and Design for Test (DFT) features.• Enhance compact device models. |
| 60 | <ul style="list-style-type: none">• Build Integrated Development Environment (IDE) for EDA tool chain and improve user Interface.• Develop hybrid integration capability to include non-SCE elements• Establish interface to system integration and analysis tools.• Improve device and process simulation tools with better fidelity and speed. |

A complete list of milestones will be provided in the BAA.



Overview of Metrics

- **Scale**
 - Number of JJs or gates and higher clock speed with increasing number of JJs
- **Quality of results**
 - Functional accuracy (no error at targeted/ideal operational zone/regime)
 - Timing accuracy (acceptable range of skew/delay, tighten as progress)
 - Accuracy of device and circuit parameters
 - Circuit area, power consumption and operation margin
 - Optimization: trade-offs (timing vs. area costs, logic gate vs. transmission performance)
- **Speed**
 - Figure of merit = cycle run time X number of cycles X functioning weight factor
 - Reference to average performance of first-phase results and/or CMOS tools
- **Flexibility**
 - Support of open/interoperable input and output standards
 - Support of multiple logic families and biasing schemes
 - Support of multiple timing/clocking schemes
 - Support of interfacing with non-SCE components



Metrics for Overall Design Capability

Milestone	Figure of Merit	Phase I	Phase II	Phase III
SCE design capability				
Model design RISC Processors or circuits of similar complexity.	Design complexity target (# of JJs)	10^5	10^6	10^7
	Clock frequency (GHz)	20	50	100
	Processor bit size	32-bit	32/64-bit	64-bit

Design target examples:

- RISC-V: Z-scale, Rocket, BOOM, etc. (32-/64-bit),
- OpenRISC OR1200 (32-bit),
- LEON3 (32-bit),
- Amber (32-bit), or
- OpenSPARC: T1, T2 (32-/64-bit).



Metrics for Logic/Digital Design and Synthesis

	Figure of Merit	Phase I	Phase II	Phase III
SCE Logic Design and Synthesis				
Develop HDL/RTL-level simulators	% of design cycle-time	< 20%	< 10%	< 5%
	% of errors in HDL simulations	0%	0%	0%
Develop Automated Logic Synthesis tool.	% of timing error in clock skew and path-to-path delay vs targets (Synthesis)	< 10%	< 5%	< 1%

Logic/digital design examples (full cores and/or functional units):

- RISC-V (Z-scale, Rocket, BOOM, etc.)
- OpenRISC OR1200,
- LEON3,
- Amber,
- OpenSPARC T1/T2.



Metrics for Circuit/Analog Design and Synthesis

Milestone	Figure of Merit	Phase I	Phase II	Phase III
SCE Circuit/Analog Design and Synthesis				
Develop circuit simulation and automated layout synthesis tools with timing and current biasing constraints, and develop timing, yield and power analysis tools; and integrate physics-based models into circuit simulators in a scalable manner.	Capacity of circuit simulators	> 10 ⁴ JJs, or 1k gates	> 10 ⁵ JJs, or 10k gates	> 10 ⁶ JJs, or 100k gates
	% of error in timing prediction with respect to a reference simulation	< 5%	< 2%	< 1%
	% of error in gate performance prediction for a given amount of fab process variation	< 5%	< 2%	< 1%
	% of error in prediction of circuit electromagnetic environment	< 5%	< 2%	< 1%
Develop Yield, Margin and Power Analysis tools				

Circuit/Analog design examples:

- Key functional units of the reference processor cores, or
- Test circuits provided by T&E teams.

Note: the scale of analog circuit (schematic) simulations need not cover the full system. The metric is set to be 1/10x of the overall target system size in terms of # of JJs or gates.



Metrics for Physical Design and Verification

Milestone	Figure of Merit	Phase I	Phase II	Phase III
SCE Physical Design and Verification				
Build tools to automate placement and routing, and to optimize circuit layout with targeted timing tolerance; and develop verification tools.	Reduction of design cycle time (benchmarked at Phase I)	Benchmark Reference (averaged)	2x	4x
	P&R timing tolerance (skew/delay variance)	< 10%	< 5%	< 2%
	% of error in extracting parameters (L, R, C) wrt a reference design structure	< 5%	< 2%	< 1%
	Reduction in layout area and interconnect length (circuit area) (P&R Optimization benchmarked at Phase I)	Benchmark Reference (averaged)	> 10%	> 20%

Physical design:

- Key functional units of the reference processors, or
- Test circuits provided by T&E teams.



Metrics for TCAD and Parameter Extraction

Milestone	Figure of Merit	Phase I	Phase II	Phase III
SCE TCAD Simulations				
Build tools to simulate device dynamics and process flow to establish cell library for synthesis and to extract model parameters for logic and circuit simulations.	% of error in predict device dynamics	< 10%	< 5%	< 1%
	% of error in process flow simulations	< 10%	< 5%	< 1%
	Run time in reference to CMOS tools	< 10x	< 5x	< 2x

Reference processes:

- MIT-LL SFQ-5ee or advanced processes, or
- Other processes provided by T&E Teams.



Metrics for Tool Features

Milestone	Figure of Merit	Phase I	Phase II	Phase III
Tool Feature				
Flexibility of EDA tool chain and TCAD tools.	Support of open/interoperable input and output standards	-	required	required
	Support of multiple logic families and biasing schemes	-	required	required
	Support of multiple timing/clocking schemes	required	required	required
	Support of interfacing with non-SCE components	-	optional	required



GFI/GFE

- GFI data for generic Standard Cell Library
 - PDKs from MIT-LL (SFQ5ee or newer),
 - Examples of basic cells from the RSFQ seedling programs, and
 - PDKs and basic cells from the C3 program when available.
- GFI contains only basic cells listed and early-stage process data.
- Performers are to generate **generic** Standard Cell Library with proposed templates from GFI and/or public domain data.
- Fab-assisted calibrations of models and TCAD tools are targeted to be developed in Phase II.



MIT-LL Process Nodes

Fabrication Process Attribute		Units	Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ7ee	SFQ8ee
Critical current density		MA/m ²	100	100	100	100	100	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (300)	700 (300)	500 (200)	500 (200)
Nb metal layers		-	4	8	8	10	10	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (500)	250 (300)	180 (220)
	Other layers	nm			500 (700)	500 (700)	350 (500)	250 (300)
Metal thickness		nm	200	200	200	200	200	150
Dielectric thickness		nm	200	200	200	200	200	180
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (700)	500 (700)	500 (500)	350 (350)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	-	-	3 - 10	3 - 10	3 - 10	3 - 10
High kinetic inductance layer		pH/sq	-	-	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (500)	500 (350)	500 (350)	350 (250)	350 (200)
Via type, stacking		-	Etched, Staggered	Etched, Stacked \2/	Etched, Stacked \2/	Etched, Stacked \2/	Stud, Stacked	Stud, Stacked
Early access availability		-		2014-09	2015-09	2016-03	2016-09	2017-09

- Nb/Al-AIOx/Nb JJ technology
- 200 mm Si wafers, full planarization



IP Status of SCE Logic Families

- The US government currently has government purpose rights to
 - Efficient-Rapid-Single-Flux-Quantum-Logic (ERSFQ), and
 - Efficient-Single-Flux-Quantum-Logic (eSFQ).
- Public domain
 - Rapid-Single-Flux-Quantum-Logic (RSFQ), and
 - Adiabatic-Quantum-Flux-Parametron-Logic (AQFP).



SuperTools Test and Evaluation

- Validation of technical claims via independent verification by T&E teams as government representatives
 - Functional verification on outputs of logic/digital design tools for selected processor soft-cores and functional units against reference implementations,
 - Validation of analog circuit design tools and verification on outputs of schematic simulators for selected (large) test circuits against known circuits and circuit simulators,
 - Verification and cross-check of physical layout of selected test circuits,
 - Validation of layout parameter/parasitic extraction tools on selected test circuits, and
 - Validation of device models and process models of test units.
- Performer site visits and demonstration of tools.

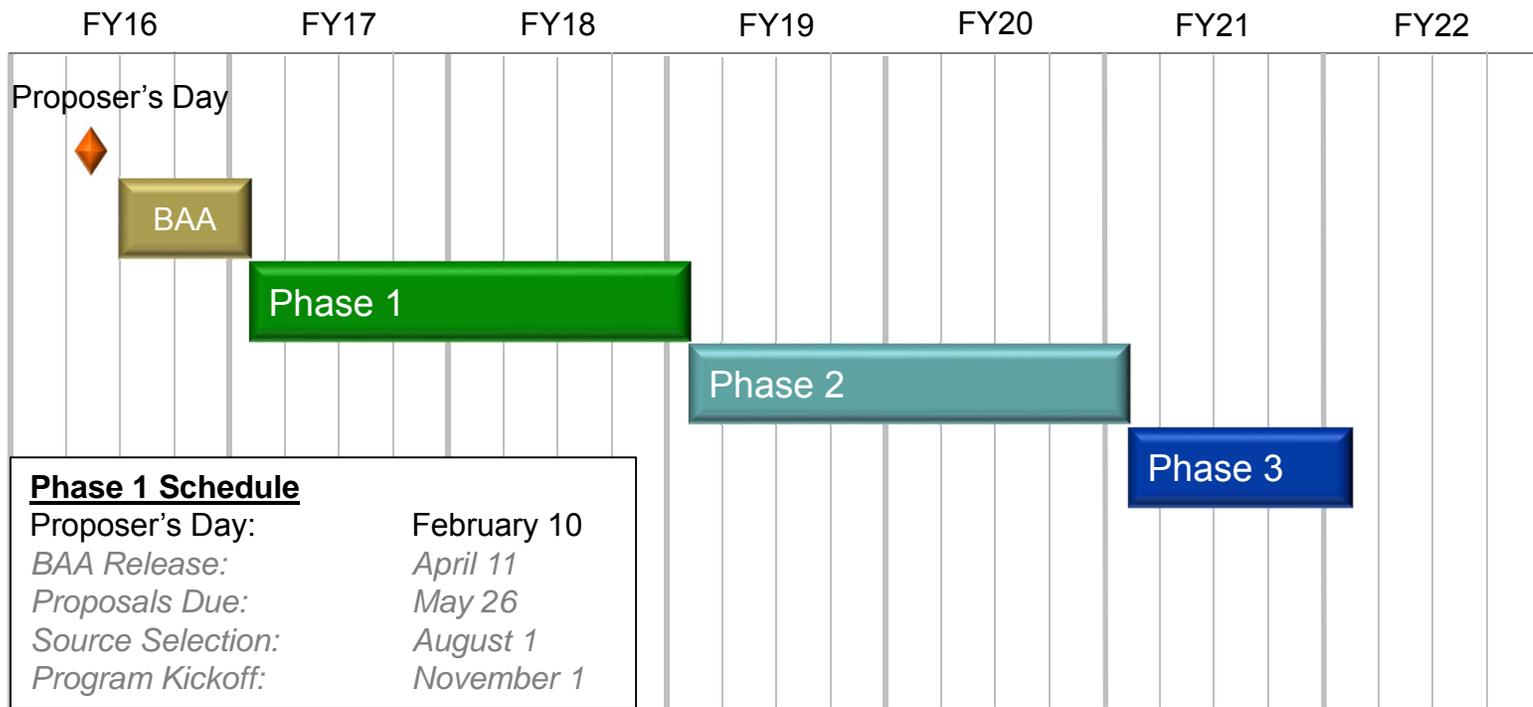


Reporting Requirements

- Monthly technical report – highlight progress from past month and plans for next month.
- Monthly financial report – form will be provided.
- Program kick-off meeting – first month of program.
- Annual performer site visit – beginning of each program year.
- Technical Exchange Meetings.
- Semi-annual Program Review Meetings.
- Test Plans
- Reports – submitted at the end of each year.



Notional/Target Schedule



BAA & Review and Source Selection



Management Plan and Teaming

- Depth and diversity will be essential to accomplish the many challenges in tool development and extension.
 - Scalability and Optimization
 - Make sure you have enough people, both from industry and academia to accomplish the goal and from proof-of-concept to large scale.
 - Sufficient resources to follow critical path while still exploring new approaches.
 - Completeness – teams should not lack any capability necessary for success, e.g. should not rely upon results or enabling technology from the community at large.
 - Tightly knit teams:
 - Clear, strong management; single point of contact.
 - No loose confederations; No teaming for teaming's sake.
 - Each team member should contribute significantly to the program goals.
 - Team members not required to participate all 5 years – consider phase transitions.



Proposal Evaluation Criteria

- Evaluation criteria in descending order of importance are:
 - Overall technical merit,
 - Effectiveness of proposed work plan,
 - Relevance to IARPA mission and SuperTools program goals,
 - Relevant experience and expertise of the members of the team,
 - Cost realism.
- All responsive proposals will be evaluated by a board of qualified government reviewers.



Summary

- SuperTools seeks to develop a comprehensive set of EDA and TCAD tools to enable VLSI design of Superconducting Electronics.
- SuperTools proposals must address all primary focus areas:

Logic/Digital Design and Synthesis

HDL/RTL simulators and logic synthesis tools

Circuit/Analog Design and Synthesis

SPICE simulator, schematic editor and layout synthesis tools

Physical Design

Place-and-Route and extraction-verification tools

TCAD and Library

Physics-based device and process simulators, compact models, and open/interoperable cell library standards.

- ***Milestones and metrics are an indispensable part of IARPA programs.***



Point of Contact

Dr. Mark I. Heiligman

Program Manager

IARPA, Safe and Secure Operations Office
Office of the Director of National Intelligence
Intelligence Advanced Research Projects Activity
Washington, DC 20511

Phone: (301) 851-7432

Fax: (301) 851-7672

Electronic mail: dni-iarpa-baa-16-03@iarpa.gov
(include IARPA-BAA-16-03 in the Subject Line)

Website: www.iarpa.gov

Questions? Please fill out cards.



Questions?

OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE



Doing Business with IARPA

Mr. Tarek Abboushi

February 10, 2016



Doing Business with IARPA - Recurring Questions

- Questions and Answers (<http://www.iarpa.gov/index.php/faqs>)
- Eligibility Info
- Intellectual Property
- Pre-Publication Review
- Preparing the Proposal (Broad Agency Announcement (BAA) Section 4)
 - Electronic Proposal Delivery (<https://iarpa-ideas.gov>)
- Organizational Conflicts of Interest
(<http://www.iarpa.gov/index.php/working-with-iarpa/iarpas-approach-to-oci>)
- Streamlining the Award Process
 - Accounting system
 - Key Personnel
- IARPA Funds Applied Research
- RECOMMENDATION: Please read the entire BAA



Responding to Q&As

- Please read entire BAA before submitting questions
- Pay attention to Section 4 (Application & Submission Info)
- Read Frequently Asked Questions on the IARPA @ <http://www.iarpa.gov/index.php/faqs>
- Send your questions as soon as possible
 - SuperTools BAA: dni-iarpa-baa-16-03@iarpa.gov
 - Write questions as clearly as possible
 - Do NOT include proprietary information



Eligible Applicants

- Collaborative efforts/teaming strongly encouraged
 - Content, communications, networking, and team formation are the responsibility of Proposers
- Foreign organizations and/or individuals may participate
 - Must comply with Non-Disclosure Agreements, Security Regulations, Export Control Laws, etc., as appropriate, as identified in the BAA



Ineligible Organizations

Other Government Agencies, Federally Funded Research and Development Centers (FFRDCs), University Affiliated Research Centers (UARCs), and any organizations that have a special relationship with the Government, including access to privileged and/or proprietary information, or access to Government equipment or real property, are not eligible to submit proposals under this BAA or participate as team members under proposals submitted by eligible entities.



Intellectual Property (IP)

- Unless otherwise requested, Government rights for data first produced under IARPA contracts will be UNLIMITED.
- At a minimum, IARPA requires Government Purpose Rights (GPR) for data developed with mixed funding
- Exceptions to GPR
 - State in the proposal any restrictions on deliverables relating to existing materials (data, software, tools, etc.)
- If selected for negotiations, you must provide the terms relating to any restricted data or software, to the Contracting Officer



Pre-Publication Review

- Funded Applied Research efforts, IARPA encourages:
 - Publication for Peer Review of **UNCLASSIFIED** research
- Prior to public release of any work submitted for publication, the Performer will:
 - Provide copies to the IARPA PM and Contracting Officer Representative (COR/COTR)
 - Ensure shared understanding of applied research implications between IARPA and Performers
 - Obtain IARPA PM approval for release



Preparing the Proposal

- Note restrictions in BAA Section 4 on proposal submissions
 - Interested Offerors must register electronically IAW instructions on: <https://iarpa-ideas.gov>
 - Interested Offerors are strongly encouraged to register in IDEAS at least 1 week prior to proposal “Due Date”
 - Offerors must ensure the version submitted to IDEAS is the “Final Version”
 - Classified proposals – Contact IARPA Chief of Security
- BAA format is established to answer most questions
- Check FBO for amendments & IARPA website for Q&As
- BAA Section 5 – Read Evaluation Criteria carefully
 - e.g. “The technical approach is credible, and includes a clear assessment of primary risks and a means to address them”



Preparing the Proposal (BAA Sect 4)

- Read IARPA's Organizational Conflict of Interest (OCI) policy:
<http://www.iarpa.gov/index.php/working-with-iarpa/iarpas-approach-to-oci>
- See also eligibility restrictions on use of Federally Funded Research and Development Centers, University Affiliated Research Centers, and other similar organizations that have a special relationship with the Government
 - Focus on possible OCIs of your institution as well as the personnel on your team
 - See Section 4: It specifies the non-Government (e.g., SETA, FFRDC, UARC, etc.) support we will be using. If you have a potential or *perceived* conflict, request waiver as soon as possible



Organizational Conflict of Interest (OCI)

- If a prospective offeror, or any of its proposed subcontractor teammates, believes that a potential conflict of interest exists or may exist (whether organizational or otherwise), the offeror should promptly raise the issue with IARPA and submit a waiver request by e-mail to the mailbox address for this BAA at dni-iarpa-baa-16-03@iarpa.gov.
- A potential conflict of interest includes but is not limited to any instance where an offeror, or any of its proposed subcontractor teammates, is providing either scientific, engineering and technical assistance (SETA) or technical consultation to IARPA. In all cases, the offeror shall identify the contract under which the SETA or consultant support is being provided.
- Without a waiver from the IARPA Director, neither an offeror, nor its proposed subcontractor teammates, can simultaneously provide SETA support or technical consultation to IARPA and compete or perform as a Performer under this solicitation.



Streamlining the Award Process

- Cost Proposal – we only need what we ask for in BAA
- Approved accounting system needed for Cost Reimbursable contracts
 - Must be able to accumulate costs on job-order basis
 - DCAA (or cognizant auditor) must approve system
 - See <http://www.dcaa.mil>, “Audit Process Overview - Information for Contractors” under the “Guidance” tab
- Statements of Work (format) may need to be revised
- Key Personnel
 - Expectations of time, note the Evaluation Criteria requiring relevant experience and expertise
- Following selection, Contracting Officer may request your review of subcontractor proposals



IARPA Funding

- IARPA funds Applied Research for the Intelligence Community (IC)
 - IARPA cannot waive the requirements of Export Administrative Regulation (EAR) or International Traffic in Arms Regulation (ITAR)
 - Not subject to DoD funding restrictions for R&D related to overhead rates
- IARPA is not DOD



Disclaimer

- This is Applied Research for the Intelligence Community
- Content of the Final BAA will be specific to this program
 - The Final BAA is being developed
 - Following issuance, look for Amendments and Q&As
 - There will likely be changes
- The information conveyed in this brief and discussion is for planning purposes and is subject to change prior to the release of the Final BAA.



QUESTIONS ?