EDA for SCE Proposer Information

- Name of Organization(s): Rensselaer Polytechnic Institute (RPI), Troy, NY 12180
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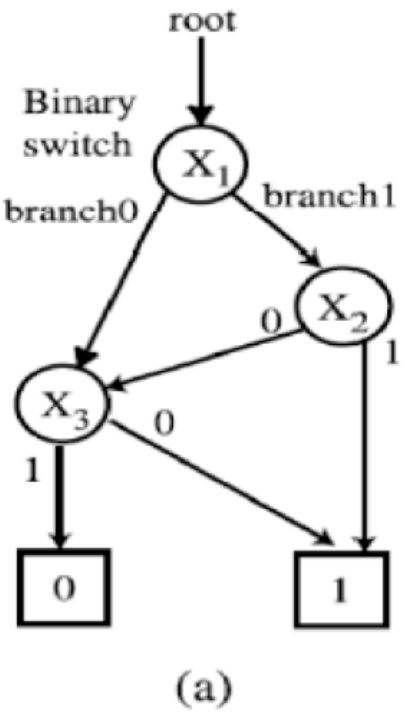
RESEARCH AREAS OF INTERERST

- Development of Josephson Junction Standard Cell Library for CADENCE ENCOUNTER auto place and route tools.
- Provision for hand crafted BIG BLOCKS in CADENCE ENCOUNTER (exploit GENUS).
- Emphasis on Asynchronous Binary Decision Diagram (BDD)
- Cell design for strong timing resiliency.
- Development of all-CADENCE oriented tool suite to handle all EDA for SCE.
- EDA for Handling special problems for JJ design like Flux Trapping.
- ARM and/or MIPS RISC architectures

Unique Qualifications

- Subcontractor to IBM IARPA C3 contact.
- SPECTRE JJ ckt simulations with VERILOG-A
- COWBOY incorporated into SPECTRE
- Margin Evaluation
- INDUCTEX interfaced to SPECTRE back annotation.
- VIRTUOSO working with MITLL design rules
- SFQ.HDL for catching mistimed pulse arrivals
- VERILOG behavioral to structural translation.
- ENCOUNTER autoplace and route from structural HDL

Research Thrusts - Standard Cells for Asynchronous BDD - Reduces timing skew



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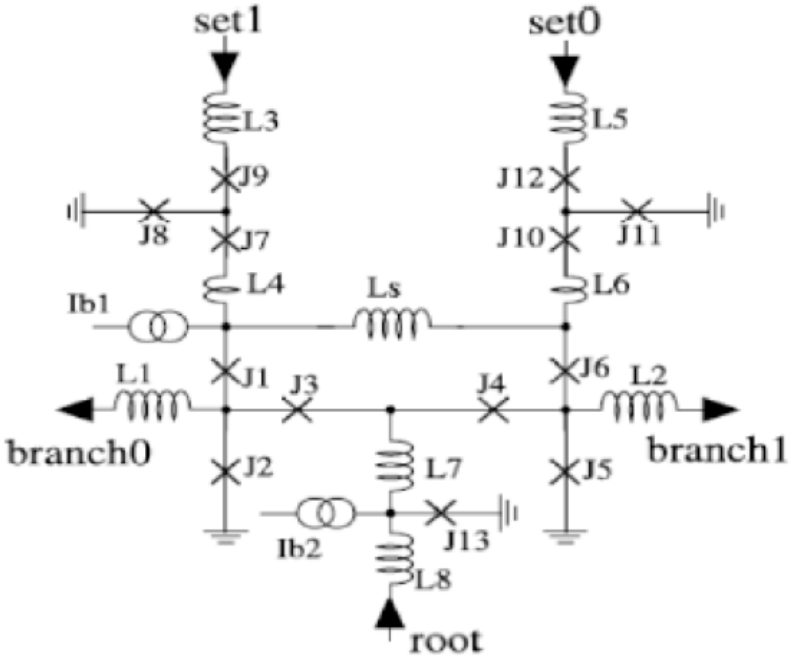

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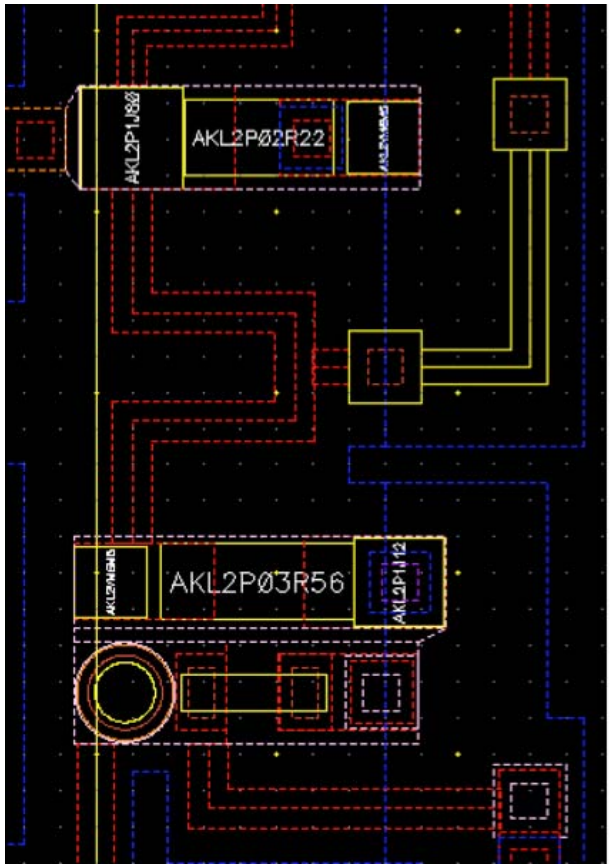

GOAL – Automate JJ RISC Design - MIPS or ARM using CMOS tools