- Lead Investigator: Adam Datesman
- Current Team Members
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  - Anna Herr
  - Quentin Herr
- Contact Information
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- Briefly describe research areas of interest
  - Reciprocal Quantum Logic (RQL) Circuit Development
- Summarize your unique qualifications and capabilities
  - Developer and System Integrator of Super Conducting Electronics
  - End customer of Tools

Background: Custom vs Digital Flow

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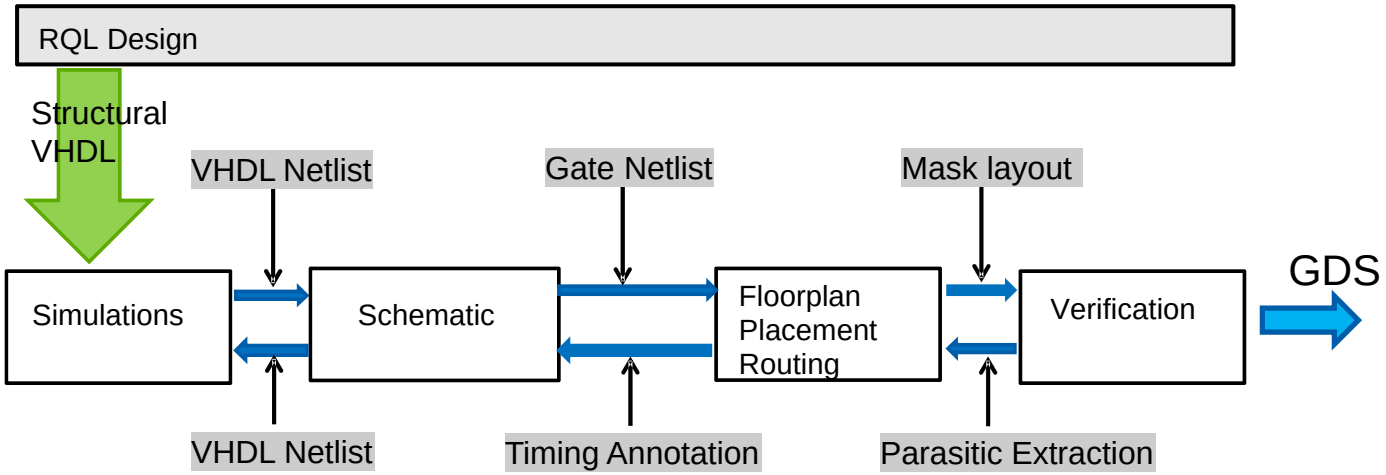
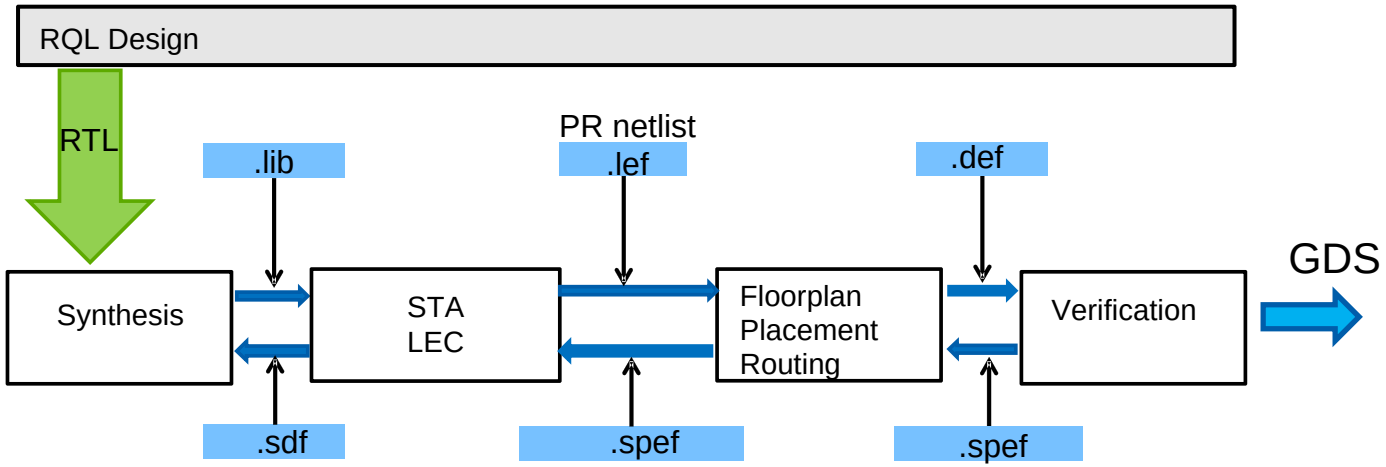
Custom



Digital



Automated flows for VLSI require different formats and libraries than custom design!

Capabilities: Synthesis & Timing Analysis

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Tool Requirements

- Synthesis, Static Timing Analysis (STA), and Logic Equivalence Checking (LEC)
- Without commercial market investment special tools for SCE are not feasible
- It is possible to use current tools by formalizing superconducting technology similar to CMOS

Challenges

- These tools require not only timing-awareness, but phase awareness
- Placement-aware synthesis
  - Fast superconducting circuits have a problem covering distance
  - Inductance interconnects do not cover distance
  - PTL interconnects require a driver and receiver
  - Without a priori knowledge of placement, timing optimization may not converge

Synthesis and static timing analysis tools must have requirements and scoping defined for reciprocal quantum logic (RQL) so that COTS tools may support SCE for scaling!

Capabilities: Placement & Routing

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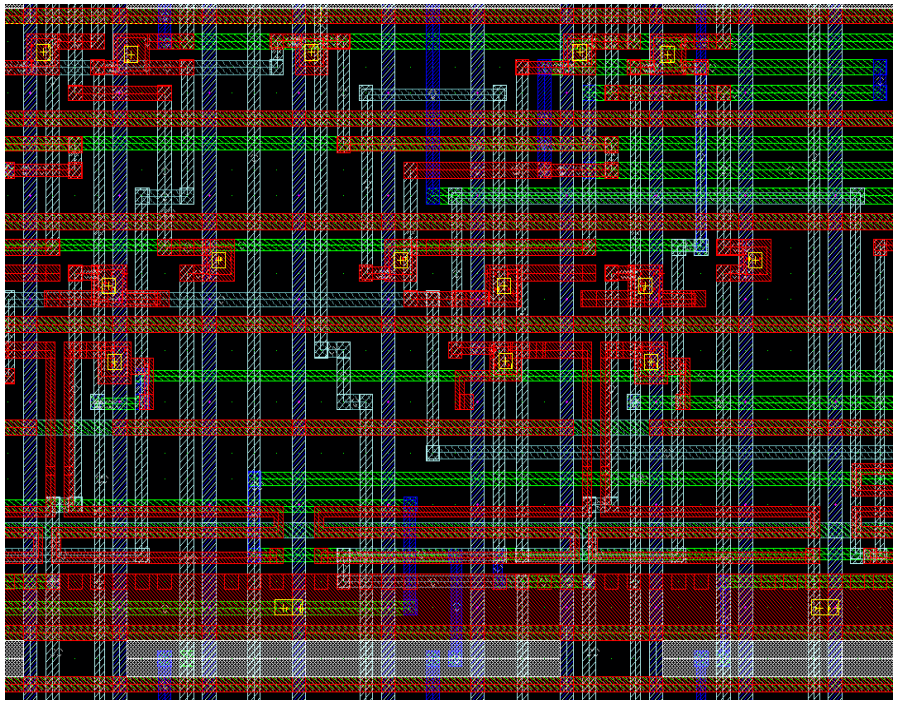
Tool Requirements

- It is possible to change RQL layout style to satisfy requirements of current digital tools

Standard cell layout on grid	->	RQL standard gates on grid
XY routing	->	RQL XY routing
Sufficient routing layers	->	RQL requires at least 4 wiring layers to close

Challenges

- Physical synthesis requires phase and timing optimization to converge
- CMOS placement algorithms do not understand fixed-value inductive constraints
- Inductance interconnects do not cover distance
- JTLs are not placed instances
- Moats and ground plane create blockage



Physical synthesis needs to optimize both timing and phase requirements while satisfying fixed inductance interconnect for VLSI scaling!

Capabilities: Verification & TCAD

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Tool Requirements

- **Verification**
  - Design Rule Check (DRC) and Layout Versus Schematic (LVS) tools
  - Electrical Rule Check (ERC) and custom rule checks
- **TCAD**
  - Standard and custom tools available for physical simulation and inductance modeling

Challenges

- Large scale extraction is required for scaling of LVS verification of all design interconnect
- Some verification requirements exist outside of the conventional signoff tools (LEC, STA, DRC, LVS, ERC).
- Frequently changing process requires a modular-compiled PDK
- Frequent innovation results in changing design constraints

Large scale extractor required for scalability of RQL circuits!
Current COTS verification tools are largely usable out-of-the-box for RQL circuits!


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