Cypress Foundry Solutions
Overview

Dr. Brad Ferguson
Wafer Foundry Services Business Development
baf@cypress.com; 952-851-5190
www.cypress.com/go/foundry
MINNESOTA PRODUCTION FAB 4

Fab:
- 200mm Equipment
- 80k ft² Cleanroom
- Class 10 + SMIF
- Onsite Wafer Probe
- 86K ML/Wk Capacity

Site:
- Bloomington, MN
- 14.7 Acres
- Room to Expand

Staff:
- ~400 employees
- QA, ENG, Yield, Defect, FA, R&D, Test, Ops, Planning

- Trusted Fab Category 1A
- 90nm-350nm Baseline Flows in Production
- Manufacturing at Consumer Scale Volumes
- Development access to Production Environment
- Develop & Manufacture D-Wave Quantum Computer IC’s


## FOUNDRY ENGAGEMENT MODELS

### Standard Foundry

- Leverage Cypress Standard Process Technologies
  - 90nm to 0.65um, Mixed signal, Nonvolatile Memory
- Manufacturing at Consumer-Scale Volumes:
  - >1B PSoC’s made in Minnesota
- Prototyping Services
  - Mask Layer Sharing for Reduced Reticle Costs
  - MPW Service also Available
  - IP available (free) on MPW runs

### Custom Foundry

- Develop in a Production Foundry:
  - Leverage Baseline Systems & Tools
  - Yield Stability & Cost Control
  - Ramp to Production w/o Transfer
- Support for Nonstandard Elements
  - Vanadium, Niobium, Platinum, Germanium, Carbon Nanotubes…
- Custom Flow Examples:
  - Superconducting Microelectronics
  - Custom ROIC Flow
  - MEMS-based Microbolometer for IR Optical Interconnect Technology
SPECIALTY FOUNDRY

D-Wave: Quantum Computing
Low-temp processing
Unique metals for cryo operation (mK)
  Pt, Nb processing
Novel integration & processing
Low-power Supercomputing apps
Low-noise detection apps

DRS: Uncooled IR Imaging
MEMS-based microbolometer
Polyimide processing capability
Low-temp processing developed
Unique sensor material: VOx
  Support for customer-owned tooling

Defense Applications
ROIC Custom Process Fabrication
  Cryo FET models, W pixel contacts,
  Topside Planarization
CNT (Carbon NanoTube) electronics
Whole-wafer imager
CIS CMOS Image Sensor

Other Applications
DNA processing/sequencing platforms
III/V & Si Heterogeneous Integration
Ultralow-power implantable electronics
Fused silica substrate processing
Rolling lithography & SFIL templates
Quick-turn custom SOC designs
SPECIALTY FAB METRICS

Focus on Cycle Time to Improve Time to Learning

- Superconducting process flow requires some dedicated tooling; focus on uptime and automation to improve cycle time
- Example: 5-layer interconnect+via flow would take ~16 days for 10 masking layers
- Excellent Yields: http://www.dwavesys.com/blog/2014/06/quantum-manufacturing

Fab Cycle Time (Days per Mask Layer)  Experiment Process Cycle Time

FAST EXPERIMENTATION WITH SHORT CYCLE TIME