OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE

# Rapid Analysis of Various Emerging Nanoelectronics (RAVEN) Proposers' Day

**Carl E. McCants, Ph. D.**
**Program Manager**
**25 August 2015**

INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)

# Agenda

| Time | Topic | Speaker |
|---|---|---|
| 8:00am – 8:30am | Welcome and Introductions | Dr. Carl McCants<br>Program Manager, IARPA |
| 8:30am – 9:00am | IARPA Overview and Remarks | Dr. Jason Matheny<br>Director, IARPA |
| 9:00am – 10:00am | RAVEN Program Overview | Dr. Carl McCants<br>Program Manager, IARPA |
| 10:00am – 10:30am | Break | |
| 10:30am – 11:00am | Doing Business With IARPA | Mr. Tarek Abboushi<br>IARPA Acquisitions |
| 11:00am – 11:30am | RAVEN Program Questions & Answers | Dr. Carl McCants<br>Program Manager, IARPA |
| 11:30am – 1:00pm | No-Host Lunch | |
| 1:00pm – 2:00pm | 5-minute Capability Presentations | Attendees<br>(**No Government**) |
| 2:00pm – 3:00pm | Networking and Teaming Discussions | Attendees<br>(**No Government**) |

# Proposers' Day Goals

- Familiarize participants with IARPA's interest in research in rapid imaging of state-of-the-art microelectronic integrated circuits.
- Familiarize participants with IARPA's mission and how to do business with IARPA.
- Provide answers to participants' questions.
  - This is your chance to alter the course of events.
- Foster discussion of synergistic capabilities among potential program participants, i.e., facilitate teaming.
  - Take a chance – someone might have a missing piece of your puzzle.

# Disclaimer

- This Proposers' Day Conference is provided solely for information and planning purposes.
- The Proposers' Day Conference does not constitute a formal solicitation for proposals or proposal abstracts.
- Nothing said at Proposers' Day changes the requirements set forth in a Broad Agency Announcement (BAA).

# Schedule

- Full proposals are due ~45 days after BAA is published.
- Once BAA is published, questions can only be submitted and answered in writing via the BAA guidance.

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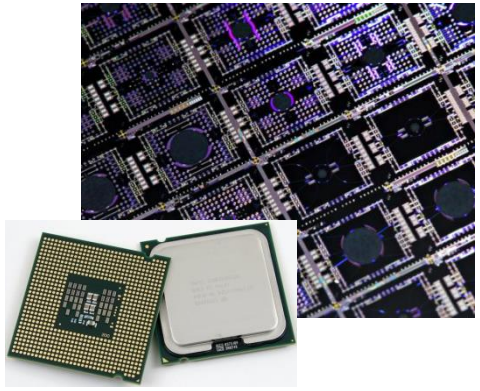
# RAVEN Overview

INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)

# How Did We Get Here?
# IARPA Circuit Analysis Tools (CAT) Program

- The IC has a wide variety of circuit development and analysis needs as covered by circuit edit, fault isolation, logic analysis, fast imaging and sample preparation for front-side, backside and stacked chip analysis.
- Analysis tools, instrumentation, and methods have not kept pace with shrinking semiconductor process geometries as captured by Moore's Law.
- Success in the CAT program will have extensive impact on the circuit analysis capability of the IC:
  - Advance the analysis techniques and technologies to address the analysis of circuits at the 22 nm technology node and below.
  - Allow our transition partners to have first access to the prototype tools, and help establish the analysis tool infrastructure to serve the user community.
  - Ensure the analysis roadmap keeps pace with Moore's Law, facilitating the development of future circuits at the 22 nm technology node and below.



# CAT Program Thrust Areas

- **Thrust 1: Circuit Edit** - Develop new approaches or techniques to cut and/or create new connections through precise deposition and removal of circuit materials to modify the electrical behavior of an integrated circuit.

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- **Thrust 4: Fast Imaging** - Develop tools capable of imaging minimum size circuit features on an entire silicon die, either a partially processed die or complete die with layers removed and sample preparation innovations to enable these advancements.

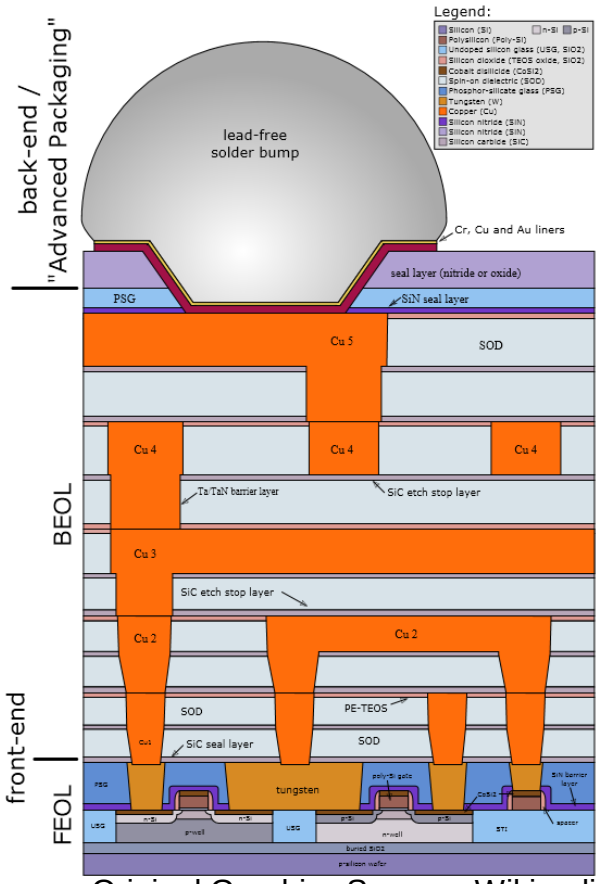
# CAT Program Thrust Areas

No imaging capabilities developed!

- **Thrust 4: Fast Imaging** - Develop tools capable of imaging minimum size circuit features on an entire silicon die, either a partially processed die or complete die with layers removed and sample preparation innovations to enable these advancements.

# RAVEN Summary (What, Why, and How)

- Characterization of integrated circuits for manufacturing verification or failure analysis often requires imaging multiple layers of the device under test.
- The current process using electron or optical microscopes is typically limited to single layer examination.
- RAVEN will reduce the time to acquire images by >100X and enable analysis of 3-D integrated circuits through:
  - Minimally- or non-destructive volumetric imaging.
  - In-situ image verification to minimize reworks.



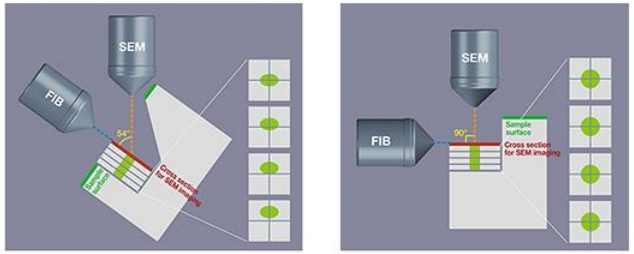

Original Graphics Source: Wikipedia

**Volumetric imaging & advanced algorithms for rapid analysis**

# Current State-of-the-art Process

- Scanning Electron Microscope (SEM) with high-resolution stage movement
  - Collect groups of images from each metal layer and via layer.
    - Etch either from front or back of wafer to reveal next metal or via layer.
  - Acquisition speed depends on number of pixels per minimum feature size, time per image.

Real-time 3D Analytical FIB-SEM Composite Instrument NX9000

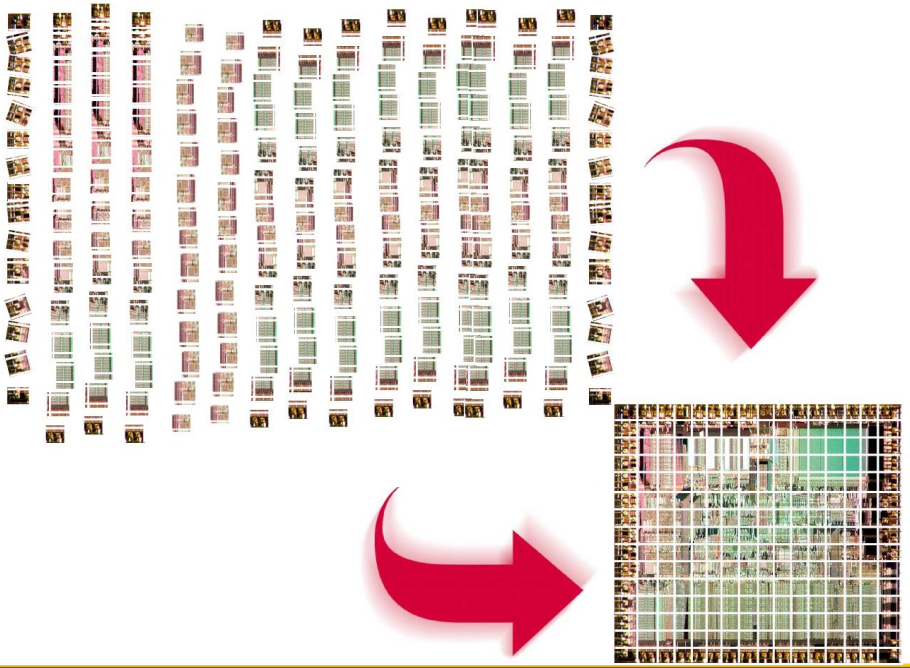



Comparison of Conventional FIB-SEM and Orthogonally-arranged FIB-SEM

Source: Hitachi

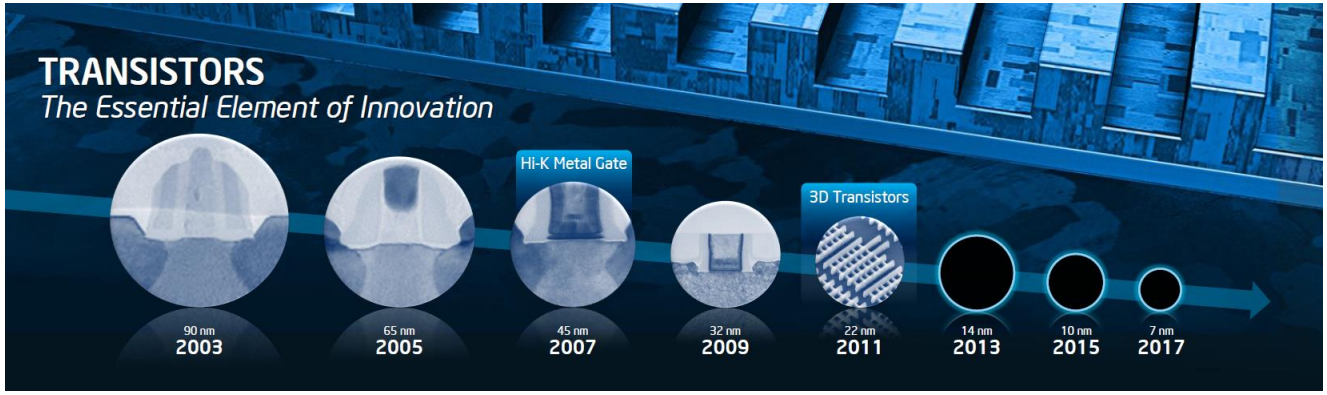
# Initial Image Analysis

- Assemble collection of images into single layer.
- Check layers for discontinuities, imaging errors, or machine errors – re-take images as needed.
- Register layers to each other.

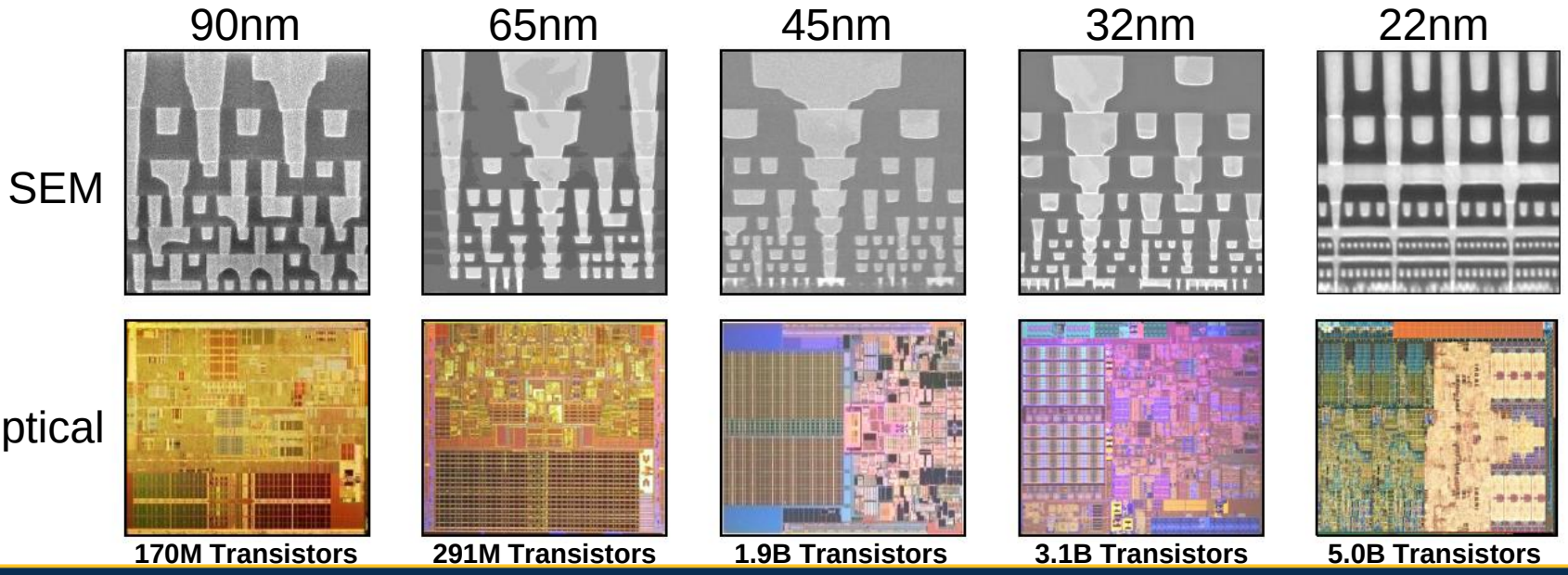


# What are the challenges?

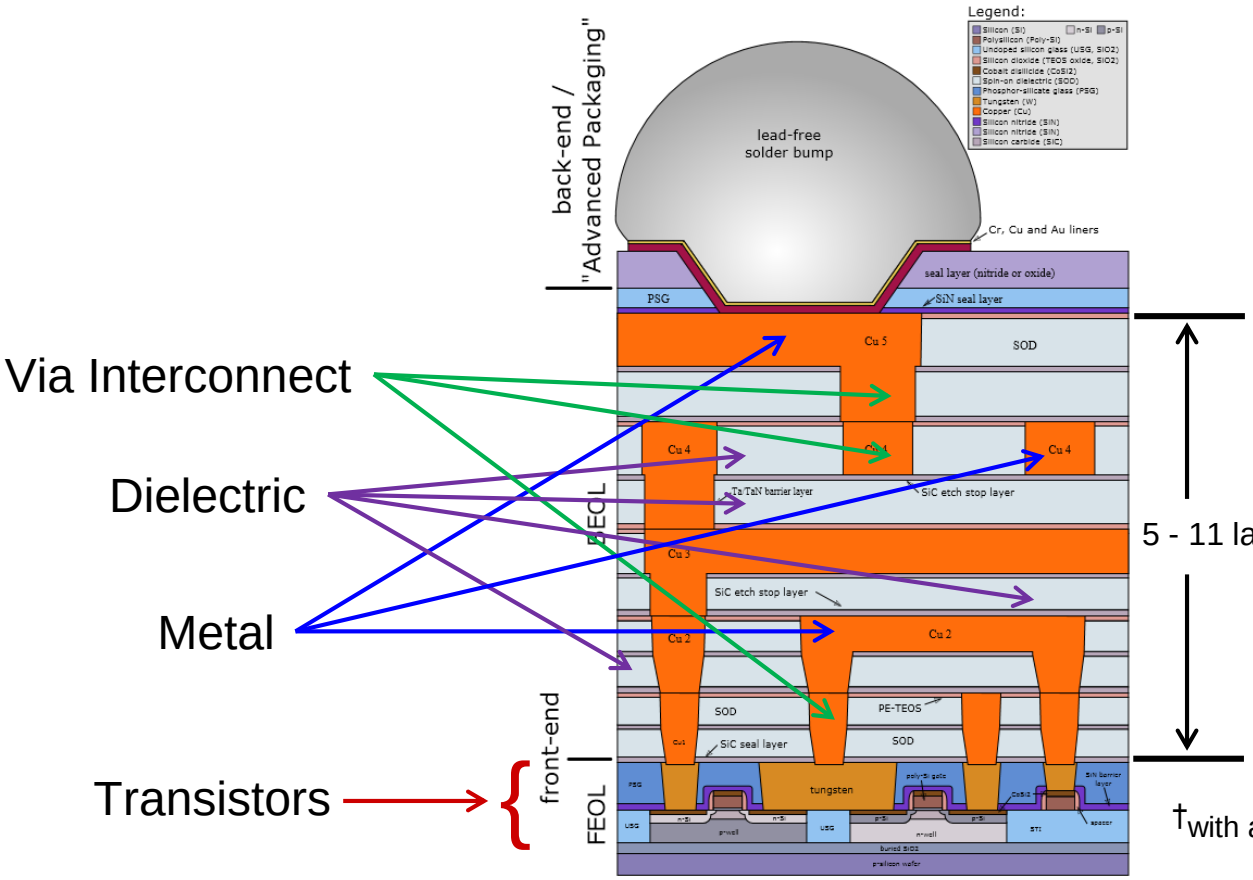
# Integrated Circuit Complexity




Source: Intel



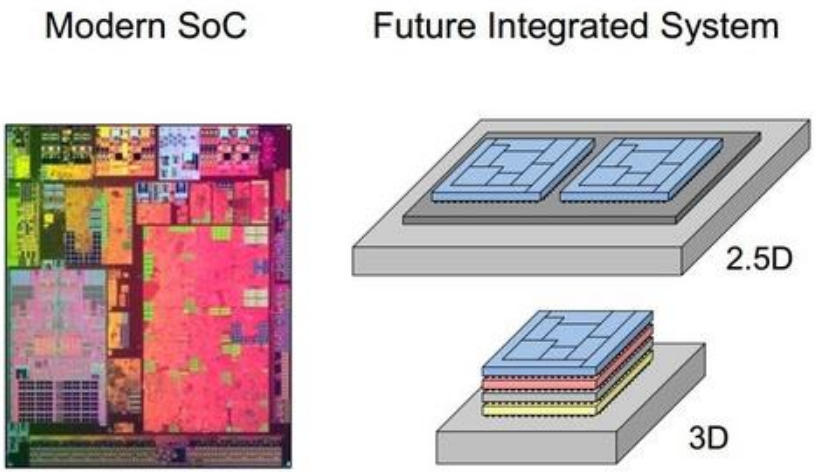
# Integrated Circuit Complexity




Original Graphic Source: Wikipedia

# Integrated Circuit Complexity

2.5-Dimensional and 3-Dimensional Integrated Circuits, and Systems-on-Chip

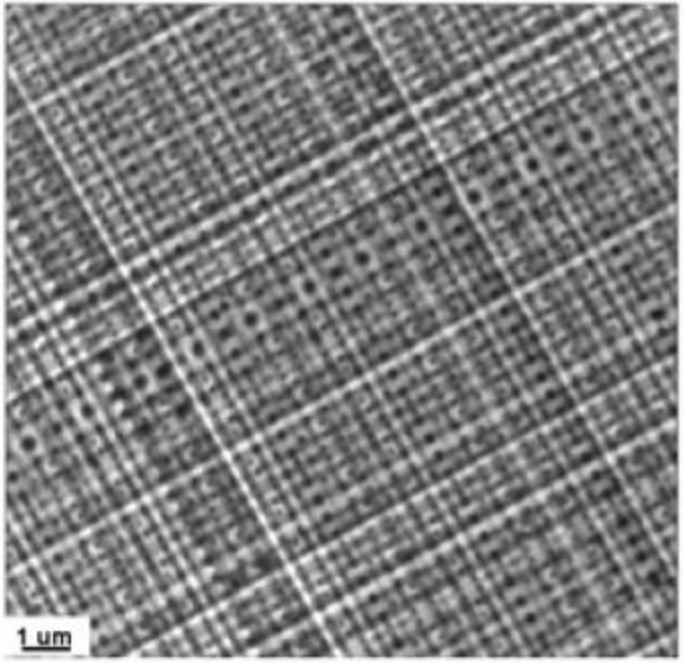


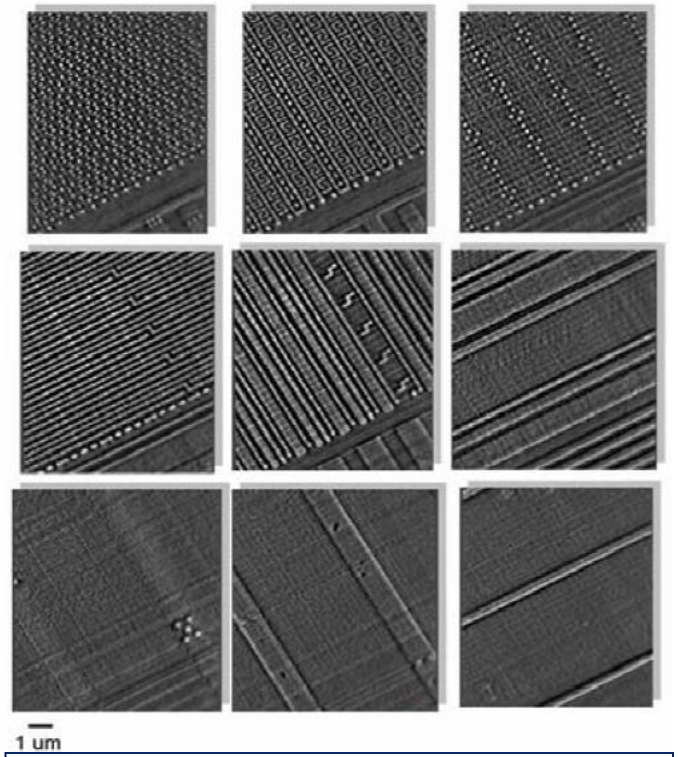

Source: Intel

# What is New?

**Replace iterative layered 2D imaging with 3D imaging scan and real-time image checks**

Source: S. Lau, et. al., “Non Destructive Failure Analysis Technique With a Laboratory Based 3D X-ray Nanotomography System”, LSI Testing Symposium 2006, Osaka, Japan



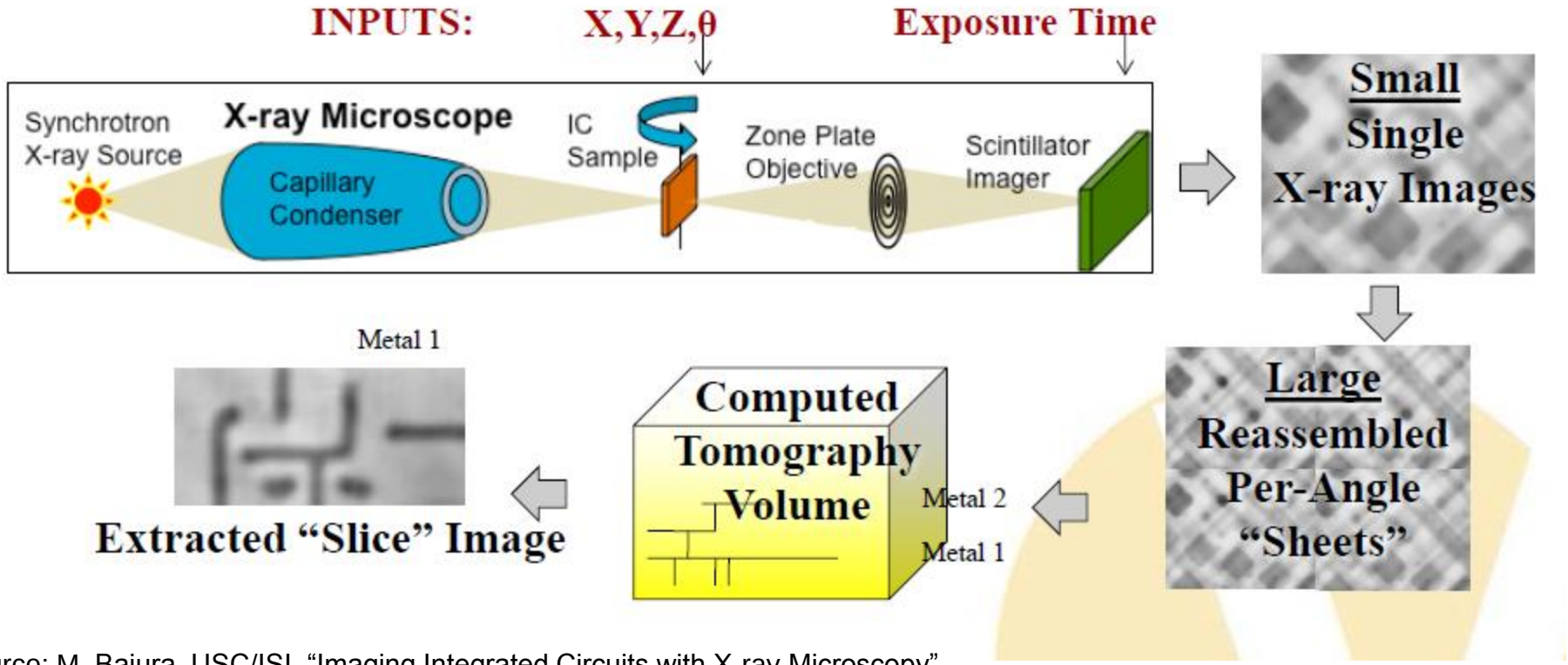




**Volumetric Image**

**Virtual Delayering**

# Enabling Technologies (1)

X-Ray Computed Tomography (CT) on a 90nm chip – DARPA TRUST Program




Source: M. Bajura, USC/ISI, "Imaging Integrated Circuits with X-ray Microscopy"

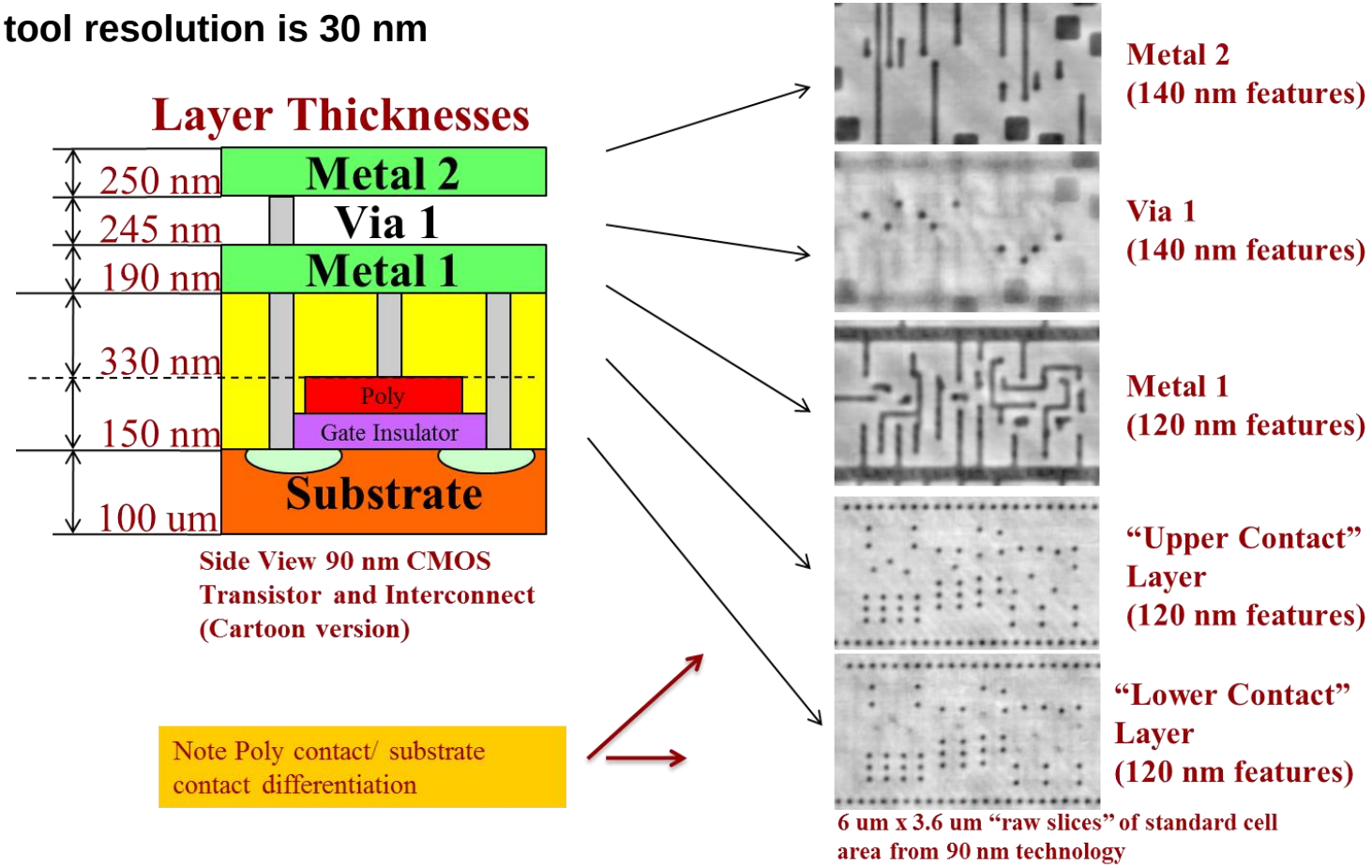
**Microscope resolution improved from 30 nm in 2011 to 10 nm in 2014**

**Image acquisition time limited by x-ray flux and number of angles per CT**

# Enabling Technologies (1)

X-Ray Computed Tomography (CT) on a 90nm chip – DARPA TRUST Program

**DARPA tool resolution is 30 nm**

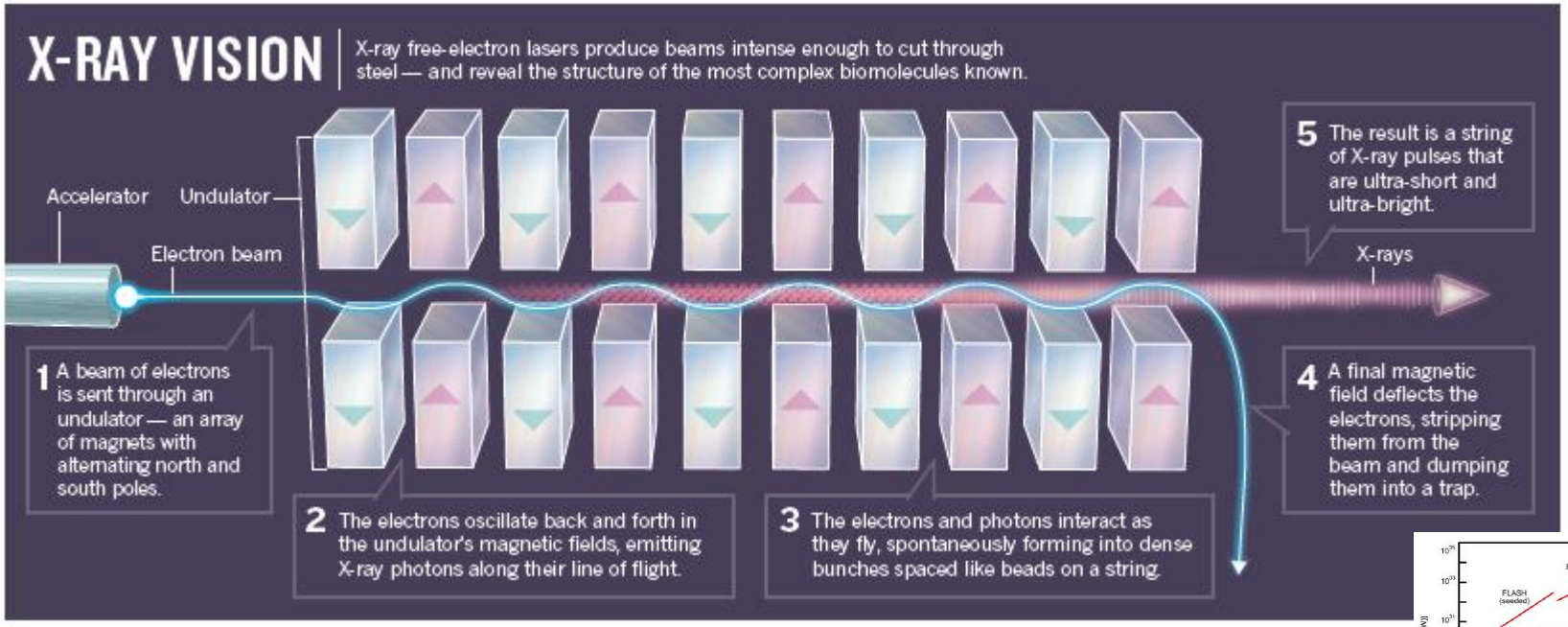



Source: M. Bajura, USC/ISI, "Imaging Integrated Circuits with X-ray Microscopy"

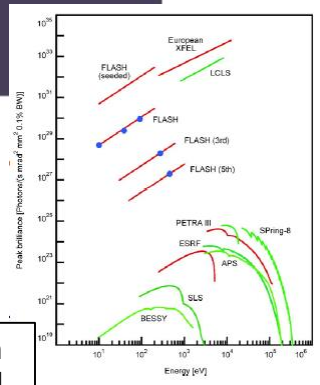
# Enabling Technologies (2)

## High-Resolution XFEL Sources

XFEL = (X-ray Free Electron Laser)




**X-ray flux is a function of brightness and pulse width**

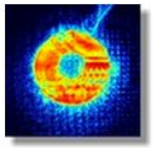



**XFEL source is one billion times brighter than synchrotron sources**
**XFEL has pulse widths 2000 times shorter than synchrotron sources**

Source: M. Waldrop, Nature **505**, 604-606 (2014)

Source: M. Altarelli, The European X-ray Free-Electron Laser, XFEL Diagnostics and Applications, Ryn, Poland

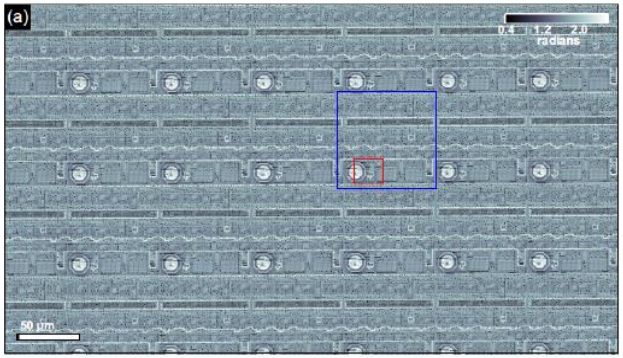
# Enabling Technologies (2)

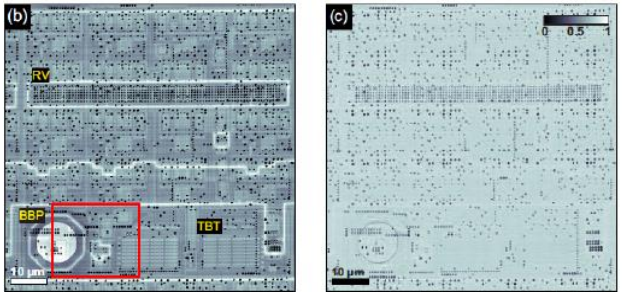


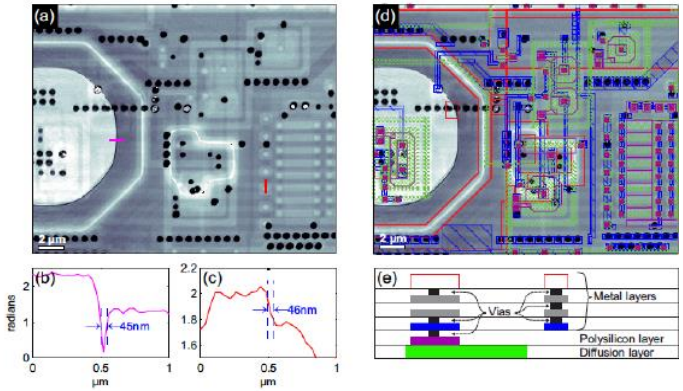
**High-throughput ptychography using Eiger: scanning X-ray nano-imaging of extended regions**

Manuel Guizar-Sicairos, Ian Johnson, Ana Diaz, Mirko Holler, Petri Karvinen, Hans-Christian Stadler, Roberto Dinapoli, Oliver Bunk, and Andreas Menzel »View Author Affiliations

Source: Optics Express, Vol. 22, Issue 12, pp. 14859-14870 (2014)
http://dx.doi.org/10.1364/OE.22.014859



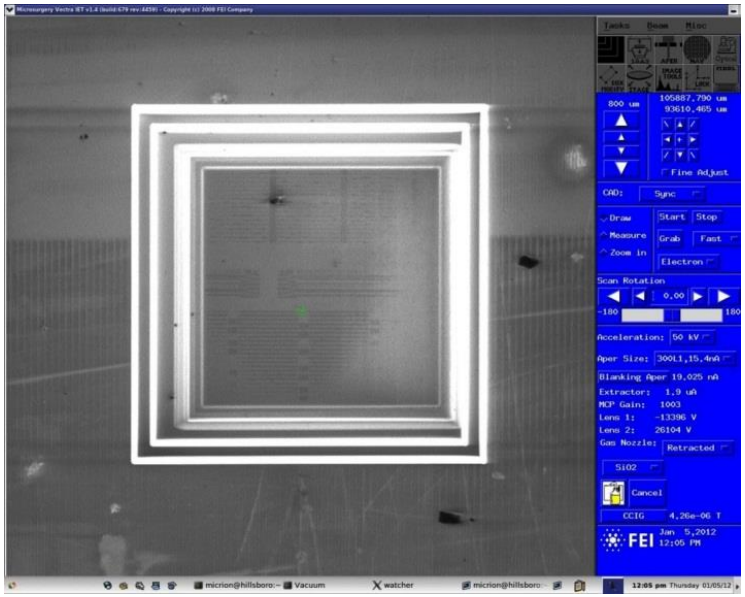



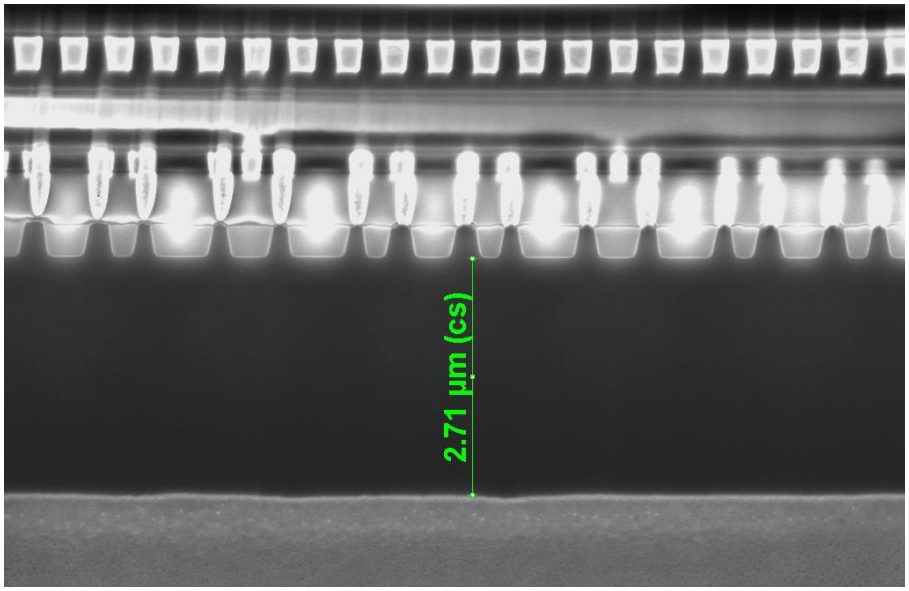

Images from 45 nm integrated circuit

# Enabling Technologies (3)

Source: Varioscale, Inc.



Circuit imaging




Analysis of transistor layer

Under the IARPA CAT program, tools were developed that can uniformly thin the substrate of devices to ~ 3 microns.

# Enabling Technologies (4)

## Compressive Sensing Techniques

Contents lists available at SciVerse ScienceDirect

Journal of Colloid and Interface Science

www.elsevier.com/locate/jcis

Feature Article

### A new approach to the investigation of nanoparticles: Electron tomography with compressed sensing

John Meurig Thomas [a,*], Rowan Leary [a,*], Paul A. Midgley [a], Daniel J. Holland [b]

[a] Department of Materials Science and Metallurgy, University of Cambridge, Pembroke Street, Cambridge CB2 3QZ, UK
[b] Department of Chemical Engineering and Biotechnology, University of Cambridge, New Museums Site, Pembroke Street, Cambridge CB2 3RA, UK

### Sparse imaging for fast electron microscopy

Hyrum S. Anderson*[1], Jovana Ilic-Helms[2], Brandon Rohrer[1], Jason Wheeler[1], Kurt Larson[1]

Sandia National Laboratories†
[1]P.O. Box 5800, Albuquerque, NM 87185
[2]P.O. Box 969, Livermore, CA 94551-0969



- Within 2 digits (in MSE) with $\approx 2.5\%$ of coeffs
- Original image = $f$, $K$-term approximation = $f_K$

$$\|f - f_K\|_2 \approx .01 \cdot \|f\|_2$$

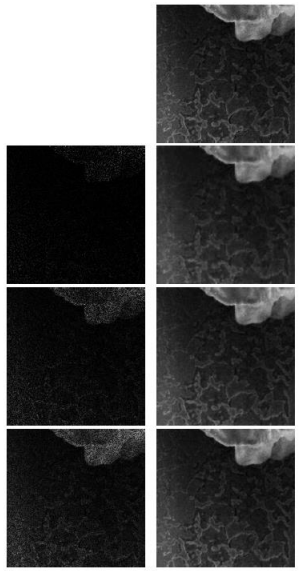


Fig. 4. (top) Original section of a high-SNR micrograph from our SEM of a particle atop the surface Gibeon meteorite slice; (2nd row) simulated 10% sparse samples (left) and reconstruction (right); (3rd row) simulated 30% sparse samples (left) and reconstruction (right); (4th row) simulated 50% sparse samples (left) and reconstruction (right)

# BAA Overview
## Test & Evaluation, GFE

# RAVEN Goal

- Develop techniques and a prototype tool to image, preferably non-destructively, all layers of a 14 nm integrated circuit chip while meeting the following requirements:
  - Image acquisition time: $\leq$ 25 days.
  - Tool resolution: $\leq$ 10 nm.
  - Analysis area: ~1 $cm^2$ .
  - Total number of samples: $\leq$ 5

# BAA Highlights

- Single BAA for all phases (base and four option periods).
- Each proposal must address all of program requirements, no partial proposals, such as development of specific component technology, will be accepted.
- The government anticipates that proposals submitted under this BAA will be unclassified.
- Multiple awards are expected.
- Foreign participants and/or individuals may participate to the extent that such participants comply with any necessary Non-Disclosure Agreements, Security Regulations, Export Control Laws and other governing statutes applicable under the circumstances.
- Option award based on performance against milestones, mission needs, and availability of funds.

# RAVEN Program At-A-Glance

| Metric | Phase 1 | Phase 2 | Phase 3 |
|---|---|---|---|
| **Duration / Goal** | 24 months / Develop Test Bench Tool | 24 months / Develop Alpha Prototype | 12 months / Finalize Beta Prototype |
| **Time** [a] | 60 days to acquire images<br>20 days to reconstruct all circuit layers | 30 days to acquire images<br>10 days to reconstruct all circuit layers | 20 days to acquire images<br>5 days to reconstruct all circuit layers |
| **Resolution** | 20 nm | 10 nm | 10 nm |
| **Reproducibility** | - | - | 95% |
| **Reliability** | - | - | 100 machine cycles |
| **Test Articles** | Bare die (>14nm feature size) | Bare die (14nm feature size) | Bare die (14/10nm feature size) |

[a] For an area approximately 1 $cm^2$

# More on Program Metrics

- Evaluate the effectiveness of proposed solutions in achieving the program objectives.
- Determine whether satisfactory progress is being made to warrant continued funding of the program.
- Set bounds on the scope of effort while affording maximum flexibility, creativity, and innovation in proposing solutions to the challenge.
- Enable proposer to suggest alternate or additional metrics if appropriate to their approach (with appropriate justification).

# RAVEN Program Plan:
## Waypoints

| Month | Milestone | Deliverable |
|---|---|---|
| **Phase 1: Demonstrate Laboratory Tool/Techniques (24 months)** | | |
| **6** | Concept design and/or feasibility study completed | Report |
| **12** | Algorithm development and test-bench design complete | Report |
| **18** | Laboratory demonstration platform built | Report |
| **22** | Demonstration of laboratory tool performance | Report |

All metrics will be verified by the RAVEN T&E Team

GFE will include test articles at the appropriate technology node

# RAVEN Program Plan:
## Waypoints

| Month | Milestone | Deliverable |
|---|---|---|
| **Phase 2: Demonstrate Alpha Prototype Tool (24 months)** | | |
| **30** | Identification of improvement areas | Report |
| **36** | Algorithm modifications and prototype design complete | Report |
| **42** | Prototype demonstration platform built | Report |
| **46** | Demonstration of prototype tool | Report |

All metrics will be verified by the RAVEN T&E Team

GFE will include test articles at the appropriate technology node

# RAVEN Program Plan:
## Waypoints

| Month | Milestone | Deliverable |
|---|---|---|
| **Phase 3: Demonstrate Beta Prototype Tool with real-time checking and repeatability (12 months)** | | |
| **54** | Basic real-time checking operational | Report |
| **58** | Demonstrate real-time checking with feedback loop, repeatability and reliability | Report |

All metrics will be verified by the RAVEN T&E Team

GFE will include test articles at the appropriate technology node

# Summary

- The RAVEN goal is to develop prototype tools and techniques to image, preferably non-destructively, all layers in a 1 $cm^2$ area of a 14 nm integrated circuit chip in less than 25 days.
- RAVEN will provide the capability to image one-of-a-kind devices.
- RAVEN will provide the capability to analyze 3-D stacked integrated circuits.

# Point of Contact


- Dr. Carl E. McCants
- Program Manager
- IARPA, Office of Safe and Secure Operations
- Office of the Director of National Intelligence
- Washington, DC 20511

- Phone: 301-851-7738
- Email: dni-iarpa-baa-15-12@iarpa.gov


- (Include IARPA-BAA-15-12 in the Subject Line)
- Website: www.iarpa.gov

# Questions?