Rapid Analysis of Various Emerging Nanoelectronics (RAVEN) Proposers’ Day

Carl E. McCants, Ph. D.
Program Manager
25 August 2015
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<thead>
<tr>
<th>Time</th>
<th>Topic</th>
<th>Speaker</th>
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<tr>
<td>8:00am – 8:30am</td>
<td>Welcome and Introductions</td>
<td>Dr. Carl McCants Program Manager, IARPA</td>
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<tr>
<td>8:30am – 9:00am</td>
<td>IARPA Overview and Remarks</td>
<td>Dr. Jason Matheny Director, IARPA</td>
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<tr>
<td>9:00am – 10:00am</td>
<td>RAVEN Program Overview</td>
<td>Dr. Carl McCants Program Manager, IARPA</td>
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<tr>
<td>10:00am – 10:30am</td>
<td>Break</td>
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<tr>
<td>10:30am – 11:00am</td>
<td>Doing Business With IARPA</td>
<td>Mr. Tarek Abboushi IARPA Acquisitions</td>
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<tr>
<td>11:00am – 11:30am</td>
<td>RAVEN Program Questions &amp; Answers</td>
<td>Dr. Carl McCants Program Manager, IARPA</td>
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<tr>
<td>11:30am – 1:00pm</td>
<td>No-Host Lunch</td>
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<tr>
<td>1:00pm – 2:00pm</td>
<td>5-minute Capability Presentations</td>
<td>Attendees (No Government)</td>
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<tr>
<td>2:00pm – 3:00pm</td>
<td>Networking and Teaming Discussions</td>
<td>Attendees (No Government)</td>
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Proposers’ Day Goals

• Familiarize participants with IARPA’s interest in research in rapid imaging of state-of-the-art microelectronic integrated circuits.

• Familiarize participants with IARPA’s mission and how to do business with IARPA.

• Provide answers to participants’ questions.
  – This is your chance to alter the course of events.

• Foster discussion of synergistic capabilities among potential program participants, i.e., facilitate teaming.
  – Take a chance – someone might have a missing piece of your puzzle.
Disclaimer

• This Proposers’ Day Conference is provided solely for information and planning purposes.

• The Proposers’ Day Conference does not constitute a formal solicitation for proposals or proposal abstracts.

• Nothing said at Proposers’ Day changes the requirements set forth in a Broad Agency Announcement (BAA).
Schedule

• Full proposals are due ~45 days after BAA is published.

• Once BAA is published, questions can only be submitted and answered in writing via the BAA guidance.
RAVEN Overview
How Did We Get Here?
IARPA Circuit Analysis Tools (CAT) Program

- The IC has a wide variety of circuit development and analysis needs as covered by circuit edit, fault isolation, logic analysis, fast imaging and sample preparation for front-side, backside and stacked chip analysis.
- Analysis tools, instrumentation, and methods have not kept pace with shrinking semiconductor process geometries as captured by Moore’s Law.
- Success in the CAT program will have extensive impact on the circuit analysis capability of the IC:
  - Advance the analysis techniques and technologies to address the analysis of circuits at the 22 nm technology node and below.
  - Allow our transition partners to have first access to the prototype tools, and help establish the analysis tool infrastructure to serve the user community.
  - Ensure the analysis roadmap keeps pace with Moore’s Law, facilitating the development of future circuits at the 22 nm technology node and below.
CAT Program Thrust Areas

- **Thrust 1: Circuit Edit** - Develop new approaches or techniques to cut and/or create new connections through precise deposition and removal of circuit materials to modify the electrical behavior of an integrated circuit.
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- **Thrust 3: Logic Analysis** - Develop advanced techniques to functionally test logic states and timing of individual transistors and internal nodes of an integrated circuit (packaged or unpackaged) and sample preparation innovations to enable these advancements.
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- **Thrust 4: Fast Imaging** - Develop tools capable of imaging minimum size circuit features on an entire silicon die, either a partially processed die or complete die with layers removed and sample preparation innovations to enable these advancements.
CAT Program Thrust Areas

No imaging capabilities developed!

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RAVEN Summary (What, Why, and How)

- Characterization of integrated circuits for manufacturing verification or failure analysis often requires imaging multiple layers of the device under test.
- The current process using electron or optical microscopes is typically limited to single layer examination.
- RAVEN will reduce the time to acquire images by >100X and enable analysis of 3-D integrated circuits through:
  - Minimally- or non-destructive volumetric imaging.
  - In-situ image verification to minimize reworks.

Volumetric imaging & advanced algorithms for rapid analysis
Current State-of-the-art Process

• Scanning Electron Microscope (SEM) with high-resolution stage movement
  • Collect groups of images from each metal layer and via layer.
    - Etch either from front or back of wafer to reveal next metal or via layer.
  • Acquisition speed depends on number of pixels per minimum feature size, time per image.

Source: Hitachi
Initial Image Analysis

- Assemble collection of images into single layer.
- Check layers for discontinuities, imaging errors, or machine errors – re-take images as needed.
- Register layers to each other.
What are the challenges?
Integrated Circuit Complexity

Source: Intel
Integrated Circuit Complexity

5 - 11 layers of metal†

†with associated via and dielectric

Integrated Circuit Complexity

2.5-Dimensional and 3-Dimensional Integrated Circuits, and Systems-on-Chip

Source: Intel
What is New?

Replace iterative layered 2D imaging with 3D imaging scan and real-time image checks

Source: S. Lau, et. al., "Non Destructive Failure Analysis Technique With a Laboratory Based 3D X-ray Nanotomography System", LSI Testing Symposium 2006, Osaka, Japan
Enabling Technologies (1)

X-Ray Computed Tomography (CT) on a 90nm chip – DARPA TRUST Program

Microscope resolution improved from 30 nm in 2011 to 10 nm in 2014
Image acquisition time limited by x-ray flux and number of angles per CT

Source: M. Bajura, USC/ISI, “Imaging Integrated Circuits with X-ray Microscopy”
Enabling Technologies (1)

X-Ray Computed Tomography (CT) on a 90nm chip – DARPA TRUST Program

DARPA tool resolution is 30 nm

Source: M. Bajura, USC/ISI, “Imaging Integrated Circuits with X-ray Microscopy”
Enabling Technologies (2)

High-Resolution XFEL Sources

XFEL = (X-ray Free Electron Laser)

XRF Vision

1. A beam of electrons is sent through an undulator — an array of magnets with alternating north and south poles.
2. The electrons oscillate back and forth in the undulator’s magnetic fields, emitting X-ray photons along their line of flight.
3. The electrons and photons interact as they fly, spontaneously forming into dense bunches spaced like beads on a string.
4. A final magnetic field deflects the electrons, stripping them from the beam and dumping them into a trap.
5. The result is a string of X-ray pulses that are ultra-short and ultra-bright.

X-ray flux is a function of brightness and pulse width

** XFEL source is one billion times brighter than synchrotron sources 
** XFEL has pulse widths 2000 times shorter than synchrotron sources 

Source: M. Altarelli, The European X-ray Free-Electron Laser, XFEL Diagnostics and Applications, Ryn, Poland
Enabling Technologies (2)

High-throughput ptychography using Eiger: scanning X-ray nano-imaging of extended regions
Manuel Guizar-Sicairos, Ian Johnson, Ana Diaz, Mirko Holler, Petri Karvinen, Hans-Christian Stadler, Roberto Dinapoli, Oliver Bunk, and Andreas Menzel


Images from 45 nm integrated circuit
Under the IARPA CAT program, tools were developed that can uniformly thin the substrate of devices to \( \sim 3 \) microns.
Enabling Technologies (4)

Compressive Sensing Techniques

Sparse imaging for fast electron microscopy

Hyrum S. Anderson¹, Jovana Ilic-Helms², Brandon Rohrer³, Jason Wheeler¹, Kurt Larson¹

¹Sandia National Laboratories
²P.O. Box 5800, Albuquerque, NM 87185
³P.O. Box 969, Livermore, CA 94551-0969
BAA Overview
Test & Evaluation, GFE
RAVEN Goal

• Develop techniques and a prototype tool to image, preferably non-destructively, all layers of a 14 nm integrated circuit chip while meeting the following requirements:
  – Image acquisition time: \( \leq 25 \) days.
  – Tool resolution: \( \leq 10 \) nm.
  – Analysis area: \( \sim 1 \text{ cm}^2 \).
  – Total number of samples: \( \leq 5 \)
BAA Highlights

• Single BAA for all phases (base and four option periods).
• Each proposal must address all of program requirements, no partial proposals, such as development of specific component technology, will be accepted.
• The government anticipates that proposals submitted under this BAA will be unclassified.
• Multiple awards are expected.
• Foreign participants and/or individuals may participate to the extent that such participants comply with any necessary Non-Disclosure Agreements, Security Regulations, Export Control Laws and other governing statutes applicable under the circumstances.
• Option award based on performance against milestones, mission needs, and availability of funds.
# RAVEN Program At-A-Glance

<table>
<thead>
<tr>
<th>Metric</th>
<th>Phase 1</th>
<th>Phase 2</th>
<th>Phase 3</th>
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<tbody>
<tr>
<td><strong>Duration / Goal</strong></td>
<td>24 months / Develop Test Bench Tool</td>
<td>24 months / Develop Alpha Prototype</td>
<td>12 months / Finalize Beta Prototype</td>
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</table>
| **Time**<sup>a</sup> | 60 days to acquire images  
  20 days to reconstruct all circuit layers | 30 days to acquire images  
  10 days to reconstruct all circuit layers | 20 days to acquire images  
  5 days to reconstruct all circuit layers |
| **Resolution**     | 20 nm                                        | 10 nm                                        | 10 nm                                        |
| **Reproducibility**| -                                            | -                                            | 95%                                          |
| **Reliability**    | -                                            | -                                            | 100 machine cycles                           |
| **Test Articles**  | Bare die (>14nm feature size)                | Bare die (14nm feature size)                | Bare die (14/10nm feature size)              |

<sup>a</sup> For an area approximately 1 cm²
More on Program Metrics

• Evaluate the effectiveness of proposed solutions in achieving the program objectives.
• Determine whether satisfactory progress is being made to warrant continued funding of the program.
• Set bounds on the scope of effort while affording maximum flexibility, creativity, and innovation in proposing solutions to the challenge.
• Enable proposer to suggest alternate or additional metrics if appropriate to their approach (with appropriate justification).
## RAVEN Program Plan: Waypoints

<table>
<thead>
<tr>
<th>Month</th>
<th>Milestone</th>
<th>Deliverable</th>
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<tbody>
<tr>
<td>6</td>
<td>Concept design and/or feasibility study completed</td>
<td>Report</td>
</tr>
<tr>
<td>12</td>
<td>Algorithm development and test-bench design complete</td>
<td>Report</td>
</tr>
<tr>
<td>18</td>
<td>Laboratory demonstration platform built</td>
<td>Report</td>
</tr>
<tr>
<td>22</td>
<td>Demonstration of laboratory tool performance</td>
<td>Report</td>
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All metrics will be verified by the RAVEN T&E Team

GFE will include test articles at the appropriate technology node
### RAVEN Program Plan: Waypoints

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<tr>
<td>30</td>
<td>Identification of improvement areas</td>
<td>Report</td>
</tr>
<tr>
<td>36</td>
<td>Algorithm modifications and prototype design complete</td>
<td>Report</td>
</tr>
<tr>
<td>42</td>
<td>Prototype demonstration platform built</td>
<td>Report</td>
</tr>
<tr>
<td>46</td>
<td>Demonstration of prototype tool</td>
<td>Report</td>
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**RAVEN Program Plan: Waypoints**

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<th>Deliverable</th>
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</thead>
<tbody>
<tr>
<td>54</td>
<td>Basic real-time checking operational</td>
<td>Report</td>
</tr>
<tr>
<td>58</td>
<td>Demonstrate real-time checking with feedback loop, repeatability and reliability</td>
<td>Report</td>
</tr>
</tbody>
</table>

Phase 3: Demonstrate Beta Prototype Tool with real-time checking and repeatability (12 months)

All metrics will be verified by the RAVEN T&E Team.

GFE will include test articles at the appropriate technology node.
Summary

- The RAVEN goal is to develop prototype tools and techniques to image, preferably non-destructively, all layers in a 1 cm$^2$ area of a 14 nm integrated circuit chip in less than 25 days.
- RAVEN will provide the capability to image one-of-a-kind devices.
- RAVEN will provide the capability to analyze 3-D stacked integrated circuits.
Point of Contact

• Dr. Carl E. McCants
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  • IARPA, Office of Safe and Secure Operations
  • Office of the Director of National Intelligence
  • Washington, DC 20511

• Phone: 301-851-7738
  • Email: dni iarpa baa 15 12 iarpa gov
  • (Include IARPA BAA 15 12 in the Subject Line)
  • Website: www iarpa gov
Questions?