

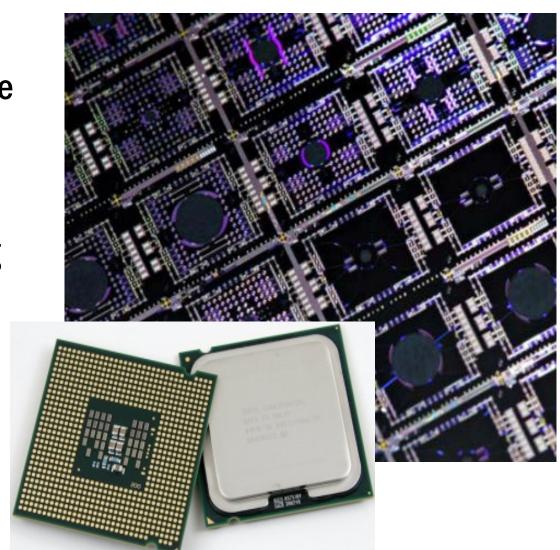
# Circuit Analysis Tools (CAT) Developing tools that keep pace with Moore's Law scaling

Program Manager: Dr. Carl McCants; E-mail: carl.mccants@iarpa.gov

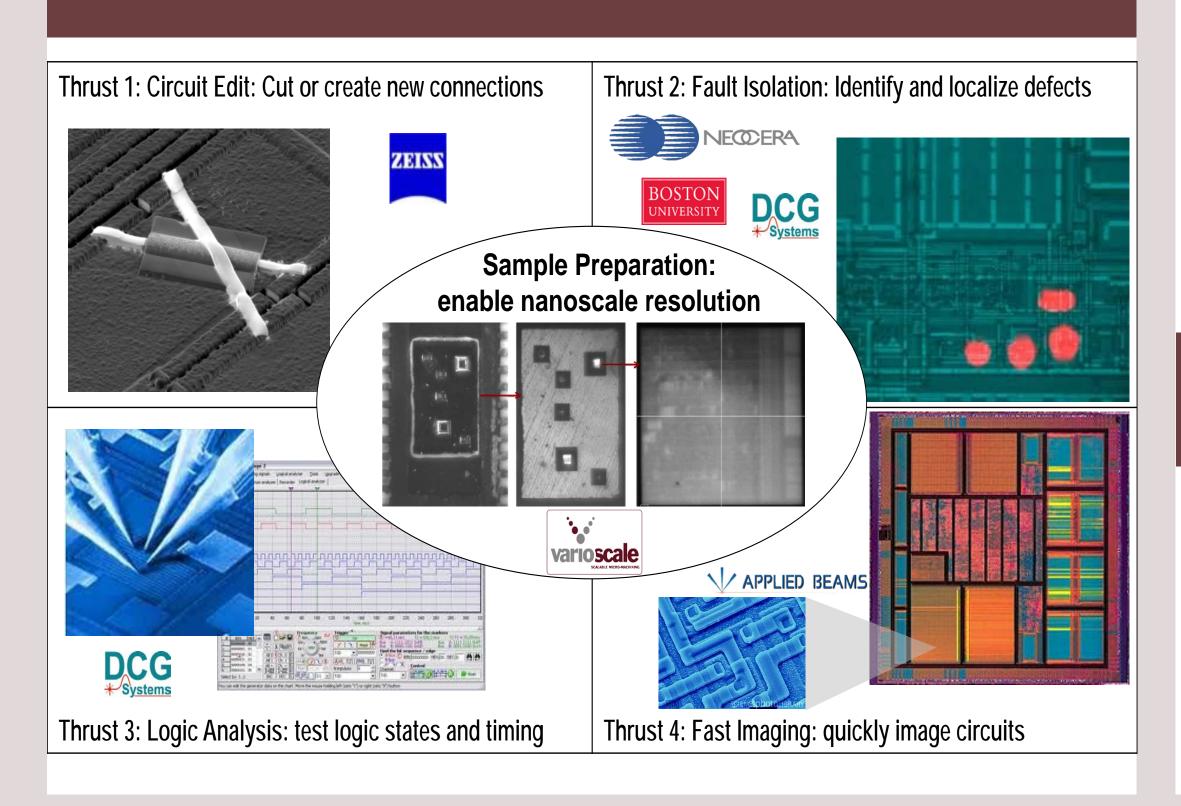


## Microelectronics designs are advancing faster than our capacity to analyze them

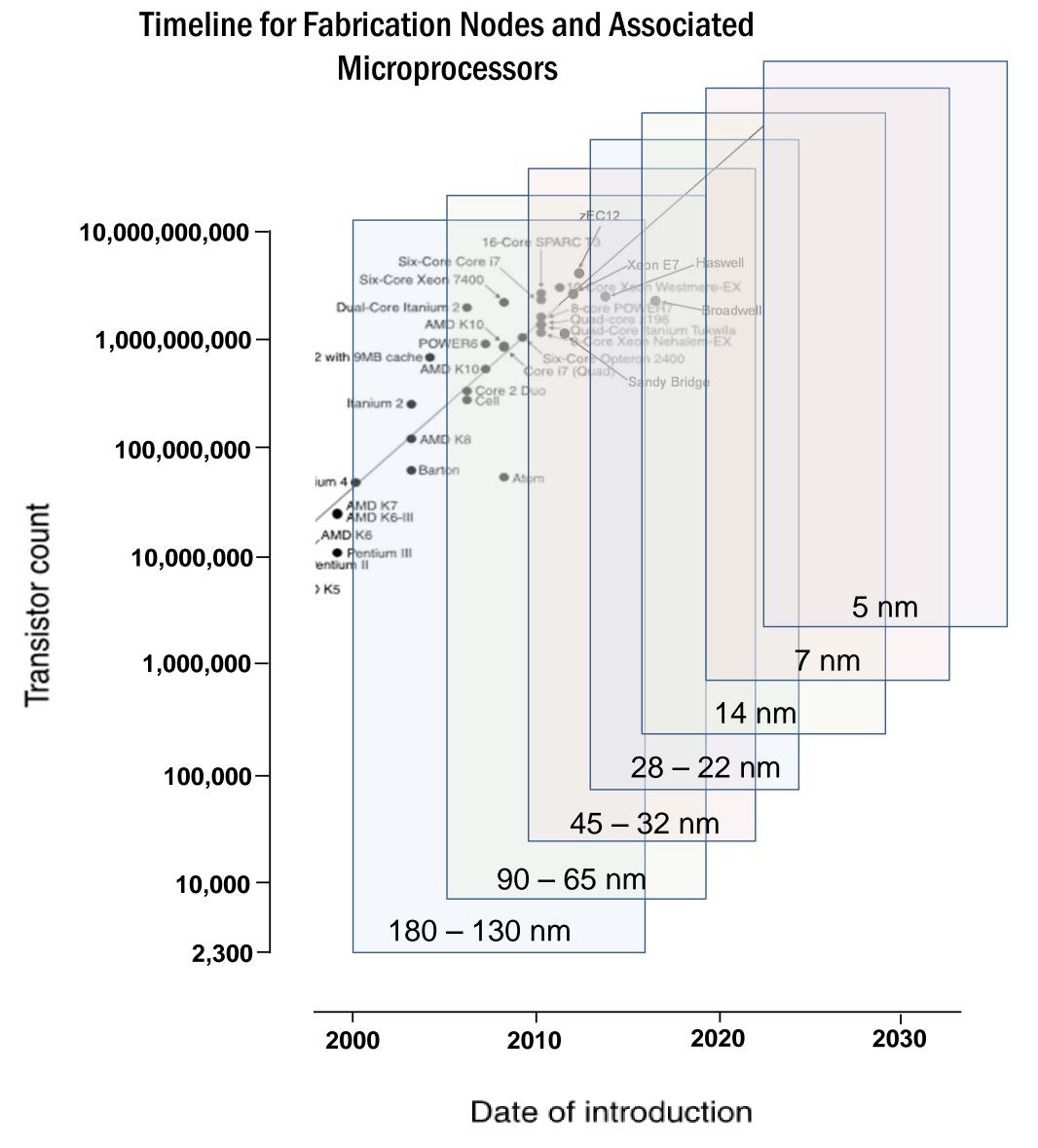
- When chips fail, whether due to a logic, timing or reliability issue, failure analysis determines the exact cause.
- Imaging and analysis tools isolate and identify the problem.
- Ideally the fix is proven by editing circuits on the prototype chip any new attempts at fabrication.



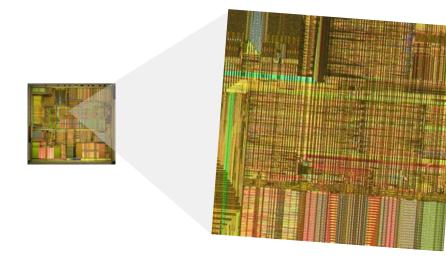
#### CAT targets each of the five major areas of failure analysis



## Before CAT, the best commercial tools could only image, probe, and edit chips at the 22nm node or higher



#### The circuits we care about are very small...



**Next generation circuits** are 10000x smaller than a human hair



## CAT leveraged the fundamental physics and chemistry of semiconductor devices to drive new tools and techniques

- First Time Resolved Emission (TRE) image at less than 0.5V.
- First two-photon Laser Assisted Device Alteration (LADA) with 100 nm resolution (vs. 300 nm in 2010).
- First demonstrated deposited metal at a linewidth of less than 10nm and a pitch of 15nm - 100 nm linewidth and 200nm pitch was state-ofthe-art in 2010.





- First demonstration of a magnetic imaging system isolating failures in a complex 3-D interconnected package with sixteen die.
- One of the world's first optical images of a 14 nm circuit.
- One of the first instances of reproducible, computer-controlled wafer thinning to less than 5 µm while maintaining uniform thickness.