

SuperTools

INTELLIGENCE VALUE

Superconductor electronics promise to enable high-speed, wideband digital signals processing and energy-efficient, high-performance computing for the U.S. Intelligence Community. The SuperTools program is developing tools to allow design and simulation of digital superconductor electronic circuits for these applications.

Superconducting electronics offers the possibility of faster and lower power circuits, but the design tools still need to be developed. The goal of the SuperTools program is to develop the first complete set of automated design tools to design and analyze complex superconducting electronic circuits. The tool chain will include standard cell libraries, process design kits, and physics-based technology computeraided design tools that enable process and device simulations, and device parameter extractions. These tools will allow automated design of complex electronic circuits, with millions of Josephson junctions—ultra-fast switches that exploit the unique physics of superconductors.

SuperTools is a five-year program that started in September of 2017. Program deliverables include EDA tools capable of designing digital circuits, with at least 10 million Josephson junctions, or 1 million logic gates. The clock frequency goal is at least 100 GHz for circuits of lower complexity.

PRIME PERFORMERS

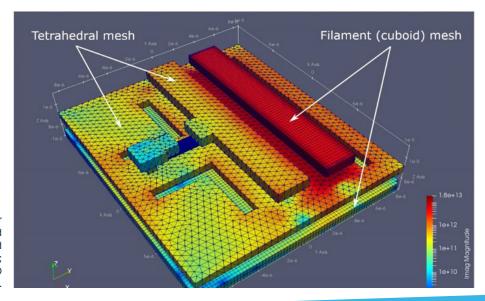
- Synopsys Inc
- University of Southern California

TESTING AND EVALUATION PARTNERS

- Massachusetts Institute of Technology Lincoln Laboratory
- Sandia National Laboratories
- National Institute of Standards and Technology
- Lawrence Berkeley National Laboratory

KEYWORDS

- Superconductor electronics
- Technology computer-aided design (TCAD)
- Josephson junctions
- Electronic design automation tools



Current flows in a superconductor circuit visualized using an advanced version of InductEx software developed during the SuperTools program; InductEx is modeling software for 3-D superconductor electronic circuits.



PROGRAM MANAGER

Pedro Espina, Ph.D. Phone: (301) 243-2089 pedro.espina@iarpa.gov



